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STUDY OF PbTe, PbSnTe, PbSe, PbSnSe, and Ge METAL INSULATOR SEMICONDUCTOR (MIS) STRUCTURES

Lawrence Michael Kost

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

Study of PbTe, PbSnTe, PbSe, PbSnSe, and Ge Metal Insulator Semiconductor (MIS) Structures

by

Lawrence Michael Kost

Thesis Advisor: T. F. Tao

March 1973

T 154585

Approved for public release; distribution unlimited.

Study of PbTe, PbSnTe, PbSe, PbSnSe, and Ge
Metal Insulator Semiconductor (MIS) Structures

by

Lawrence Michael Kost
Lieutenant, United States Navy
B.S., Pennsylvania State University, 1965

Submitted in partial fulfillment of the
requirements for the degree of

ELECTRICAL ENGINEER

from the

NAVAL POSTGRADUATE SCHOOL
March 1973

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ABSTRACT

A thorough understanding and a well developed fabrication procedure of MIS structures are the prerequisite for CCD applications. The object of this thesis is to study the narrow gap semiconductor MIS and investigate its feasibility for IR-CCI applications. Two MIS studies were made.

First, MIS of five lead-tin semiconductors were fabricated using E-gun evaporated 100-450Å thick Al_2O_3 or SiO_2 layers as insulators. C-V measurements indicated that these MIS behave qualitatively like that of Si-MOS. Accumulation, depletion and inversion layers were controlled by the gate voltage. However, comparisons of measured C-V with theoretical calculations did not yield quantitative agreement.

Second, MIS of 0.05Ω-cm p-type and 40Ω-cm n-type Ge were also studied. C-V and C-t measurements indicated standard MOS behavior although some small hysteresis was found. Analysis based on C-V data showed that the flatband voltage was approximately -1.2 volts and interface state density was on the order of $10^{13}/cm^2$.

In addition, effects of electron bombardment simulating the space environment around Jupiter on a n-channel depletion MOSFET were studied. The negative threshold voltage was decreased and at a total dose of $2X10^{15}$ e/cm^2, it became positive making the MOSFET an enhancement type of very poor quality.

TABLE OF CONTENTS

I. INTRODUCTION -- 14

II. REVIEW OF CCD CHARACTERISTICS -------------------- 20

A. CONCEPT -- 20

B. STRUCTURE -------------------------------------- 20

C. MODUS OPERANDI --------------------------------- 21

D. FIGURES OF MERIT ------------------------------- 26

1. Charge Storage Capability ---------------- 26

2. Transfer Efficiency ---------------------- 26

3. Transfer Time, t_0 ------------------------ 27

4. Storage Time, t_s ------------------------- 28

5. Charge Conservation ---------------------- 28

E. NON-INSULATOR CCD ------------------------------ 29

III. REVIEW OF MIS CHARACTERISTICS -------------------- 32

A. DESCRIPTION OF AN IDEAL MIS -------------------- 32

B. CAPACITANCE-VOLTAGE CHARACTERISTICS OF AN IDEAL MIS ------------------------------------ 38

1. Description of Typical C-V Curves -------- 38

2. Theoretical C-V Equations ---------------- 40

C. CAPACITANCE-TIME CHARACTERISTICS OF MIS ------ 42

1. Storage Time ----------------------------- 44

2. Storage Capacity ------------------------- 45

D. OTHER RELATED MIS CHARACTERISTICS ------------ 45

E. C-V CHARACTERISTICS IN REAL MIS -------------- 46

1. Physical Changes ------------------------- 46

2. Device Characteristic Changes ----------- 51

3. Theoretical Changes --------------------- 53

IV. MEASUREMENT TECHNIQUES ON MIS ------------------ 53

A. HIGH-FREQUENCY C-V ------------------------ 53

1. Basic Schematic ------------------------- 53

2. Errors Due to Leaky Insulators ---------- 55

B. C-t CURVES -------------------------------- 56

1. Basic Schematic ------------------------- 56

2. Errors Associated with C-t Measurements - 59

C. LOW-FREQUENCY C-V CURVES ------------------ 59

V. ANALYSIS OF C-V DATA ------------------------- 66

A. COMPUTER PROGRAM TO ANALYZE THE HIGH AND LOW-FREQUENCY C-V DATA ------------------------ 66

1. Semiconductor Surface and Applied Potential ------------------------------ 67

2. Interface/State Density ----------------- 69

3. Effective Interface Charge -------------- 70

B. COMPUTER PROGRAM BASED ON HIGH-FREQUENCY C-V DATA ONLY ------------------------------ 71

1. Conductivity Type ----------------------- 71

2. Interface State Density ----------------- 72

C. COMPUTER PROGRAM TO ANALYZE HIGH-FREQUENCY INVERSION MINIMUM CAPACITANCE --------------- 73

VI. PREPARATION OF MIS SAMPLES OF IV-VI SEMICONDUCTORS 75

A. $Pb_{1-X}Sn_XTe$ AND $Pb_{1-Y}Sn_YSe$ THIN FILM SEMICONDUCTORS ---------------------------- 75

B. INSULATORS -------------------------------- 76

C. METAL DEPOSITION -------------------------- 81

VII. EXPERIMENTAL RESULTS OF IV-VI ALLOY SEMICONDUCTOR MIS -- 83

A. MIS SAMPLES STUDIED ---------------------- 83

B. HIGH-FREQUENCY C-V RESULTS ---------------- 84

1. $Pb_{1-X}Sn_XTe$ MIS C-V Curves at Room Temperature ---------------------------- 84

2. $Pb_{1-X}Sn_XTe$ MIS C-V Curves at Liquid Nitrogen Temperature ------------------ 96

3. $Pb_{1-Y}Sn_YSe$ MIS C-V Curves at Room Temperature ---------------------------- 99

4. $Pb_{1-Y}Sn_YSe$ C-t Response --------------- 101

C. ANALYSIS OF MEASURED C-V DATA ------------- 107

1. Low and High-Frequency Data Analysis --- 107

2. High-Frequency Only Data Analysis ------ 108

3. Theoretical Minimum High-Frequency Capacitance Analysis ------------------ 110

VIII. EXPERIMENTAL RESULTS OF GERMANIUM MIS ---------- 114

A. DEVICE STRUCTURE ------------------------ 114

B. THEORETICAL PROCEDURE -------------------- 115

C. EXPERIMENTAL RESULTS --------------------- 118

1. High and Low-Frequency C-V ------------ 118

a. P-Type Ge-MIS --------------------- 118

b. N-Type Ge-MIS --------------------- 121

2. C-t Measurement ------------------------ 121

D. ANALYSIS OF Ge-MIS DATA ------------------ 124

1. P-Type Data Analysis ------------------ 124

2. Analysis of n-Type Ge-MIS ------------- 137

IX. EFFECT OF ELECTRON BOMBARDMENT ON SILICON N-CHANNEL DEPLETION MOSFET ---------------------- 139

A. INSRODUCTION ---------------------------- 139

B. SAMPLES --------------------------------- 139

1. Electron Bombardment ---------------------- 139

2. Experimental Results ---------------------- 142

3. Experimental Analysis --------------------- 143

4. Discussion -------------------------------- 155

X. CONCLUSION ---------------------------------- 157

COMPUTER OUTPUT -------------------------------- 160

COMPUTER PROGRAMS ------------------------------ 161

LIST OF REFERENCES ----------------------------- 170

INITIAL DISTRIBUTION LIST ---------------------- 173

FORM DD1473 ------------------------------------ 174

LIST OF TABLES

I. List of MIS Samples Prepared for Experimentation -- 80

II. $Pb_{1-X}Sn_XTe$ Semiconductor MIS Experimentally Investigated --- 84

III. $Pb_{1-Y}Sn_YSe$ Semiconductor MIS Experimentally Investigated --- 101

IV. Summary of Data Analysis Output for PbSe (Al_2O_3-100A°) MIS from Experimental High and Low-Frequency C-V ------------------------------ 108

V. Summary of High-Frequency Only Data Analysis for Four Lead-Tin Semiconductor MIS Samples ---- 109

VI. Summary of Absolute Capacitance Minima for IV-VI Semiconductor MIS ------------------------ 113

VII. Summary of Tabular Output Data for Three Different Gate Locations on Ge-MIS (p-Type) ---- 134

VIII. Summary of Tabular Output Data for Ge-MIS (n-Type) --------------------------------------- 138

IX. MOSFET e-Beam Total Accumulated Dosage Obtained 142

X. MOSFET Threshold Voltage Shift as a Function of Total Accumulated Dosage -------------------- 150

LIST OF FIGURES

2-1 Charge-Coupled Device Basic Structure and Transfer Process ---------------------------------- 22

2-2 Construction and Operation of an Ion Implantation 2ϕ-CCD -- 24

2-3 Input and Output Schemes of a CCD --------------- 25

2-4 Theoretical Conduction-Band Profile for a Double-Junction CCD ------------------------------------ 30

3-1 Energy Bands and Charge Distribution in Ideal MIS for Various Bias Conditions --------------------- 34

3-2 Expanded View of MIS Energy Band Diagram Under Inversion Conditions ---------------------------- 37

3-3 Ideal C-V Curves for p-Type MIS ----------------- 39

3-4 Accumulation to Inversion Pulsed Response of a MIS 43

3-5 Classification of Charges and States in a Non-Ideal MIS -- 47

3-6 "Finger Prints" of Non-Ideal MIS ---------------- 50

3-7 MIS Equivalent Circuit -------------------------- 52

4-1 Block Diagram for High-Frequency C-V, and C-t Measurements ------------------------------------- 54

4-2 Leaky Insulator Effect on n-Type Si-MOS with Insulator Resistance Greater than 1MΩ ------------ 57

4-3 Leaky Insulator Effect on p-Type Ge-MIS with Insulator Resistance of 10KΩ -------------------- 58

4-4 Block Diagram for Low-Frequency and G-V Measurements ------------------------------------- 60

4-5 Equivalent Circuit for Low-Frequency Phase Sensitivity Measurements ------------------------ 62

6-1 MIS Thin-Film Sample --------------------------- 77

7-1 Theoretical C-V Curve for PbTe MIS (Ideal),
$N = 1X10^{18}$ cm^{-3},
T = 300°K
Insulator: Al_2O_3 (100A°) ---------------------- 85

7-2 Theoretical C-V Curve for $Pb_{.80}Sn_{.20}Te$ MIS (Ideal),
$N = 1X10^{18}$ cm^{-3}, T = 300°K,
Insulator: SiO_2 (450A°) ---------------------- 86

7-3 Experimental C-V Curve for PbTe MIS,
T = 300°K,
Insulator: Al_2O_3 (100A°) ---------------------- 87

7-4 Experimental C-V Curve for PbTe MIS,
T = 300°K,
Insulator: SiO_2 (450A°) ---------------------- 88

7-5 Experimental C-V Curve for $Pb_{.82}Sn_{.18}Te$ MIS,
T = 300°K,
Insulator: Al_2O_3 (300A°) ---------------------- 89

7-6 Experimental C-V Curve for $Pb_{.80}Sn_{.20}Te$ MIS,
T = 300°K,
Insulator: Al_2O_3 (100A°) ---------------------- 90

7-7 Experimental C-V Curve for $Pb_{.80}Sn_{.20}Te$ MIS,
T = 300°K,
Insulator: Al_2O_3 (300A°) ---------------------- 91

7-8 Experimental C-V Curve for $Pb_{.80}Sn_{.20}Te$ MIS,
T = 300°K,
Insulator: SiO_2 (450A°) ---------------------- 92

7-9 Experimental C-V Curve for $Pb_{.76}Sn_{.24}Te$ MIS,
T = 300°K,
Insulator: Al_2O_3 (100A°) ---------------------- 93

7-10 Experimental C-V Curve for $Pb_{.76}Sn_{.24}Te$ MIS,
T = 300°K,
Insulator: Al_2O_3 (300A°) ---------------------- 94

7-11 Experimental C-V Curve for PbTe MIS at Various Low Temperatures,
Insulator: Al_2O_3 (300A°) ---------------------- 97

7-12 Experimental C-V Curve for PbTe MIS,
T = 80°K, T = 300°K for Gate 1,
Insulator: Al_2O_3 (100A°) ---------------------- 98

7-13 Theoretical C-V Curve for $Pb_{.90}Sn_{.10}Se$ MIS (Ideal),
$N = 1X10^{18}$ cm^{-3}, T = 300°K,
Insulator: SiO_2 (450A°) ---------------------- 100

7-14 Experimental C-V Curves for PbSe #1,
T = 300°K,
Insulator Al_2O_3 (300A°) -------------------- 102

7-15 Experimental C-V Curves for PbSe MIS #2 Showing Low-Frequency Response,
T = 300°K,
Insulator: Al_2O_3 (300A°) -------------------- 103

7-16 Experimental C-V Curve for $Pb_{.97}Sn_{.03}Se$ MIS,
T = 300°K,
Insulator: Al_2O_3 (300A°) -------------------- 104

7-17 Experimental C-V Curves for $Pb_{.90}Sn_{.10}Se$ MIS,
T = 300°K,
Insulator: SiO_2 (450A°) -------------------- 105

7-18 C-t Response for $Pb_{.90}Sn_{.10}Se$ MIS,
T = 300°K,
Insulator: SiO_2 (450A°) -------------------- 106

7-19 Plots of C_{MINHF} Versus Impurity Concentration for IV-VI Semiconductor - Al_2O_3 (100A°) MIS ---- 111

7-20 Plots of C_{MINHF} Versus Impurity Concentration for IV-VI Semiconductor TiO_2 (100A°) MIS ------- 112

8-1 Theoretical C-V Curves for n-Type Ge-MIS (Ideal)
Insulator: Al_2O_3 - 180A°
N = $5X10^{13}$ cm^{-3}, T = 300°K ----------------- 116

8-2 Theoretical C-V Curves for p-Type Ge-MIS (Ideal)
Insulator: Al_2O_3 - 250A°
N = $1.3X10^{17}$ cm^{-3}, T = 300°K --------------- 117

8-3 Experimental C-V Curves for p-Type Ge-MIS Showing the Hysteresis Effect
Insulator: Al_2O_3 - 250A°,
N = $1.3X10^{17}$ cm^{-3}, T = 300°K --------------- 119

8-4 Experimental C-V Curves for p-Type Ge-MIS Showing Nonuniformity at Different Gate 1 Locations
Insulator: Al_2O_3 - 250A°
N = $5X10^{13}$ cm^{-3}, T = 300°K ----------------- 120

8-5 Experimental C-V Curves for n-Type Ge-MIS
Red: Reduced Scale Showing Hysteresis
Exp: Expanded Scale
Insulator: Al_2O_3 - 180A°,
N = $5X10^{13}$ cm^{-3}, T = 300°K ----------------- 122

8-6 Experimental High-Frequency C-V and C-t Response for Ge-MIS (p-Type)
a) C-V Response
b) C-t Response ---------------------------- 123

8-7 Experimental C-V Curves for Ge-MIS (p-Type) Gate #1 -- 125

8-8 $(C_i/C_S)^2$ - U_S Plot for Ge-MIS (p-Type) Gate #1 - 126

8-9 V_S-V_a Plot for Ge-MIS (p-Type) Gate #1 --------- 127

8-10 N_{SS} - ψ Plot for Ge-MIS (p-Type) Gate #1 ------- 128

8-11 Q_{eff} - V_S Plot for Ge-MIS (p-Type) Gate #1 ----- 129

8-12 Experimental C-V Curves for Ge-MIS (p-Type) Gate #2 -- 131

8-13 Experimental C-V Curves for Ge-MIS (p-Type) Gate #3 -- 132

8-14 $(C_i/C_S)^2$ - U_S Plot for Ge-MIS (p-Type) Gate #3 - 133

8-15 V_S-V_a Plot for Ge-MIS (p-Type) Gate #3 --------- 135

8-16 N_{SS} - ψ Plot for Ge-MIS (p-Type) Gate #3 ------- 136

9-1 I_{dS}-V_{dS} Characteristics for MOSFET before Irradiation ---------------------------- 140

9-2 C-V Characteristics for MOSFET before Irradiation ------------------------------------ 141

9-3 MOSFET I_{dS}-V_{dS} Characteristics after a Total Accumulated Dosage of $3X10^{12}$ e/cm^2 ------------- 144

9-4 MOSFET I_{dS}-V_{dS} Characteristics after a Total Accumulated Dosage of $6.3X10^{13}$ e/cm^2 ----------- 145

9-5 MOSFET I_{dS}-V_{dS} Characteristics after a Total Accumulated Dosage of $2.063X10^{15}$ e/cm^2 --------- 146

9-6 MOSFET C-V Characteristics after a Total Accumulated Dosage of $3X10^{12}$ e/cm^2 ------------- 147

9-7 MOSFET C-V Characteristics after a Total Accumulated Dosage of $6.3X10^{13}$ e/cm^2 ----------- 148

9-8 MOSFET C-V Characteristics after a Total Accumulated Dosage of 2.063×10^{15} e/cm^2 ---------- 149

9-9 MOSFET V_S-V_a Characteristics after a Total Accumulated Dosage of 3×10^{12} e/cm^2 ------------- 151

9-10 MOSFET V_S-V_a Characteristics after a Total Accumulated Dosage of 6.3×10^{13} e/cm^2 ------------ 152

9-11 MOSFET N_{SS}-V_S Characteristics after a Total Accumulated Dosage of 3×10^{12} e/cm^2 ------------- [illegible]

9-12 MOSFET N_{SS}-V_S Characteristics after a Total Accumulated Dosage of 6.3×10^{13} e/cm^2 ---------- 154

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I. INTRODUCTION

The charge-coupled device (CCD) concept was first introduced by Boyle and Smith of Bell Telephone Laboratory around March, 1970 [2]. A new device principle was propos in which the signal was represented by minority carriers in the depletion layer of a metal-oxide semiconductor (MOS structure. It is a new device concept but uses Si-MOS technology already in existence.

The development in the past three years was indeed amazing and CCD has demonstrated its major impact on three electronic areas: imaging, analog delay and memory. The influence is different in these areas, however.

(1) For imaging, the impact is major mainly because the competing imaging technologies all used, in one way or another, the relatively more complicated electron-beam scanning mechanism and high-vacuum technology of the conventional vidicons. In CCI (charge-coupled imagers), a scene incident on the MOS array surface is transformed into a distribution of minority charge packets under the gates. To read the image out, a sequence of voltage pulses are applied to the array which transfer the charge packets across the CCI and produce a video signal at the output. The device is smaller, much cheaper to build and simpler to operate.

Recently, Fairchild has reported a linear 500 element CCI array which has a 1,000 to 1 dynamic range and maintains good picture at 0.03 foot-candles.[1] (Vidicons have about a 100 to 1 dynamic range.) Such a performance is approaching the field requirement of low-light-level television (L^3TV). Bell Telephone Laboratories, using 3 CCI chips of 106 × 128 elements each, has demonstrated that CCI can be used as color TV cameras although much denser CCI are needed for practical applications (250 × 250 elements for picturephone, 550 × 550 elements for commercial TV quality) [6]. There seems to be a good probability that CCI will replace most of the electron beam scanning devices in camera tube applications. CCI can equally be used in other applications as solid state page readers, fascimile sensors, information displays, computer terminal readouts, etc.

(2) In anolog delay applications, CCD will also make an important impact replacing the present delay methods in signal processing using glass rods, quartz crystals or coaxial cables. In CCD, the signal is introduced and then transferred across the device by the clocking pulses. Delays from microseconds to milliseconds can be achieved by changing the clock frequency. For the first time, an anolog signal delay device can be fabricated by IC process and incorporated into other IC systems. The applications

---

[1] Several other companies have achieved similar results.

are numerous in communications, radar, etc., such as the delay lines in TV sets, transversal delay line filters in telephone systems for equalizing phone lines, matching filters for coding and decoding in radar systems, etc.

(3) For digital memory, the impact of CCD is not as immediate mainly because of the highly developed magnetic core and semiconductor memory technologies already in existence and the other developing memory techniques such as magnetic bubbles and optical holography. However, operational buffer memory, consisting of two 480 bit CCD shift registers on a 110 mil^2 Si chip has been demonstrated [13]. For bulk memory, gross packing density of 3 million bits per square inch was predicted. Cost of 0.01-0.1¢ per bit is possible. It is conceivable that CCD may have stronger impact in memory than in imaging and anolog delay.

The interest of this thesis is in the application of CCD in imaging, more specifically, in infrared imaging. The interest in infrared imaging is quite broad indeed, such as the downward looking and forward looking infrared systems in military and security night vision missions, remote sensing in ecology and environment fields, nondestructive testing in industrial quality control and the very promising thermography in medical diagnostics.

However, the feasibility of CCD concepts in IR had not been investigated at all at the start of this thesis (June 1972). At it stands today, several approaches have been discussed. First, the monolithic MOS approach in narrow

energy gap semiconductors similar to the Si-CCD is the obvious extension to IR. Second, semiconductors of small energy gap are used as IR sensors, and the photo-excited carriers are transferred into the Si-CCD. Two subapproaches exist, one being the photoconductive sensor-Si-CCD package and the other being the IR semiconductor-Si-CCD heterojunction approach.

This thesis considers the monolithic approach. It should be pointed out that another research program of this group, the development of polycrystalline narrow gap semiconductor photoconductive IR detectors [16][11], can be applied to the photoconductor-Si-CCD approach. In this monolithic approach, the first task is to examine if the surface layer of the new semiconductor in a MIS structure can be controlled by the gate voltage. Specifically, it is necessary to determine if:

a. Accumulation, depletion and inversion layers can be controlled by the application of proper gate voltages.

b. Does the surface layer stay long enough in its partially depleted state before it becomes inversion layer? This is the so-called storage time which must be longer than the integration time in an imaging application.

c. If the storage time is long enough, is the storage capacity adequate for handling the photon flux of a scene?

Only after these questions receive affirmative answers, can we proceed to investigate the IR CCI applications. For this purpose, a group of IV-VI compound and alloy semiconductors are studied: PbTe, PbSe, PbSnTe and PbSnSe. Their

energy gaps are all less than 0.3 ev. which make them suitable for IR imaging beyond 4μ, such as in the 4-5μ and 8-12μ atmospheric windows. MIS structures using Al_2O_3 and SiO_2 as insulators and Hg probes as metal gates were fabricated and studied.

The main purpose of this thesis is to investigate if depletion and inversion layers exist at the interface of the insulator and semiconductor in these MIS. If so, can they be controlled by the gate voltage?

During the course of this research, MIS of two other semiconductors, Ge and Si, were also studied. The motivation was to acquaint ourselves with the MIS research using MIS samples of two well known semiconductors. First, Ge-MIS using Al_2O_3 as insulators were studied. The energy gap of Ge varies from 0.67 ev at 300°K to 0.73 ev at 77°K which is suitable for 1.70μ IR imaging. It should be noted that Ge-MIS has not been studied before, making its study useful by its own right.

Second, the effect of high-energy-electron bombardment on a n-channel Si depletion MOSFET was also studied. The electron energy was 65.4 Mev. and the radiation was approximately 5×10^{11} electrons per square centimeter per second. Exposure to this radiation for five seconds is equivalent to exposure in the space environment around Jupiter for about ten hours. This study is also related to a research program at the Linear Electron Accelerator of the Naval Postgraduate

School studying the radiation effects on semiconductor devices during a space flight around Jupiter.

II. REVIEW OF CCD CHARACTERISTICS

Since the charge-coupled concept is so new, a description of the device is necessary. This section of the thesis will cover the concept, the structure, the method of operation and the "figures of merit" of the CCD.

A. CONCEPT

The basic concept of CCD's consists of storing minority carriers (or their absence) in a spatially defined depletion region (potential well) at the surface of a homogeneous semiconductor and to move this charge along the surface by moving the potential minimum. The potential minima are produced by applying a voltage to conducting electrodes (gates), formed on the surface of the insulator covering the semiconductor, and driving the surface into depletion. A variety of functions can be performed by injecting charge into the potential well, transferring this charge along the surface of the semiconductor, and detecting the charge at some output location.

B. STRUCTURE

The basic structure of a CCD is a linear array of MIS[2]

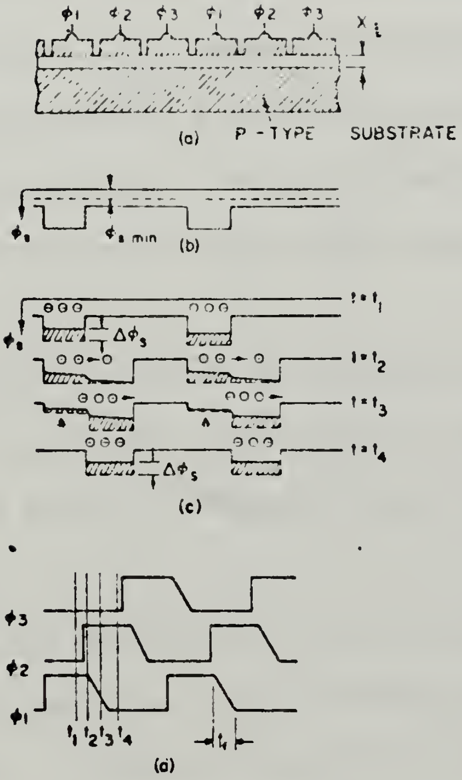
---

[2] An MIS element is a metal-insulator-semiconductor structure whose main function is to produce a potential well in the semiconductor from a bias applied between the metal and semiconductor. MIS will be covered in detail in the next chapter of this thesis.

elements as shown in Figure 2-1 [1]. Figure 2-1 also depicts the storage and transfer schemes in a CCD. In Fig. 2-1a, every third electrode is biased more strongly than the other two and charge can be stored in the potential well under gate 1. In part b., the transfer sequence, the bias on gate 2 is made greater and as a result, if the gate spacing is close enough to allow adequate coupling, the charge transfers into the region under gate 2. Part d. in Fig. 2-1 indicates the clock pulse scheme used to transfer the charge. In this case the device is a 3 phase (3ϕ) CCD since three different voltage levels are required to move the charge. Other type schemes are described below.

C. MODUS OPERANDI

The operation of the CCD is based on the minority carrier charge formation, storage, and transfer in an inversion layer at the semiconductor surface. The composite element of a CCD in the case of the 3ϕ device are 3-MIS basic elements. There are, however, other clocking schemes that are used. Note also that the charge transfer can be in any direction dependent on the nature of the voltage pulses. Inherent disadvanteges in the 3ϕ device are the criticalness of the interelectrode spacing, cross unders required in device fabrication, and the gap areas between electrodes which can assume potentials that adversely affect the transfer process.



φ1
φ2
φ3
φ1
φ2
φ3
X_i
(a)
P - TYPE
SUBSTRATE
ϕ_s
$\phi_{s\,min}$
(b)
ϕ_s
$\Delta\phi_s$
$t = t_1$
$t = t_2$
$t = t_3$
$t = t_4$
$\Delta\phi_s$
(c)
φ3
φ2
φ1
t_1 t_2 t_3 t_4
t_t
(d)

Figure 2-1. Charge-Coupled Device Basic Structure and Transfer Process: (a) Cross section of the charge-coupled structure, (b) surface potential profile at the beginning of the transfer cycle, (c) surface potential profiles during the transfer cycle, and (d) three-phase clock waveforms.

Figure 2-2 shows the construction and operation of the 2ϕ-CCD. This type CCD not only is simpler to construct than the 3ϕ but also has the advantage of minimizing the separation between electrodes. The direction of charge transfer is determined by the asymmetry of the potential wells under two adjacent electrodes; the smaller potential well beneath the thicker oxide causes the packet to flow to the right only. The asymmetric potential wells necessary to produce directionality can also be obtained with an ion implanted barrier as shown by the shaded region in Figure 2-2.

Other CCD structures include 4ϕ-CCD devices and a uniphase CCD just recently proposed [9] in which a silicon nitride layer with a built-in charge allows one-directional charge-packet flow.

The input and output schemes of the CCD are depicted in Fig. 2-3. Optical generation, the scheme most important in this thesis project, is listed in part c. of Fig. 2-3. Note that in the figure the radiation is introduced in the back of the device, through the semiconductor. Other devices pass the radiation through windows in the front. For example, Melen [17] uses polysilicon gates between aluminum gates through which the light image passes. Other devices coming into being are CCD with depleted-buried channels in which the charge packet flows. These devices will gain rapidly in popularity because of the elimination of surface states which plague surface CCD's.

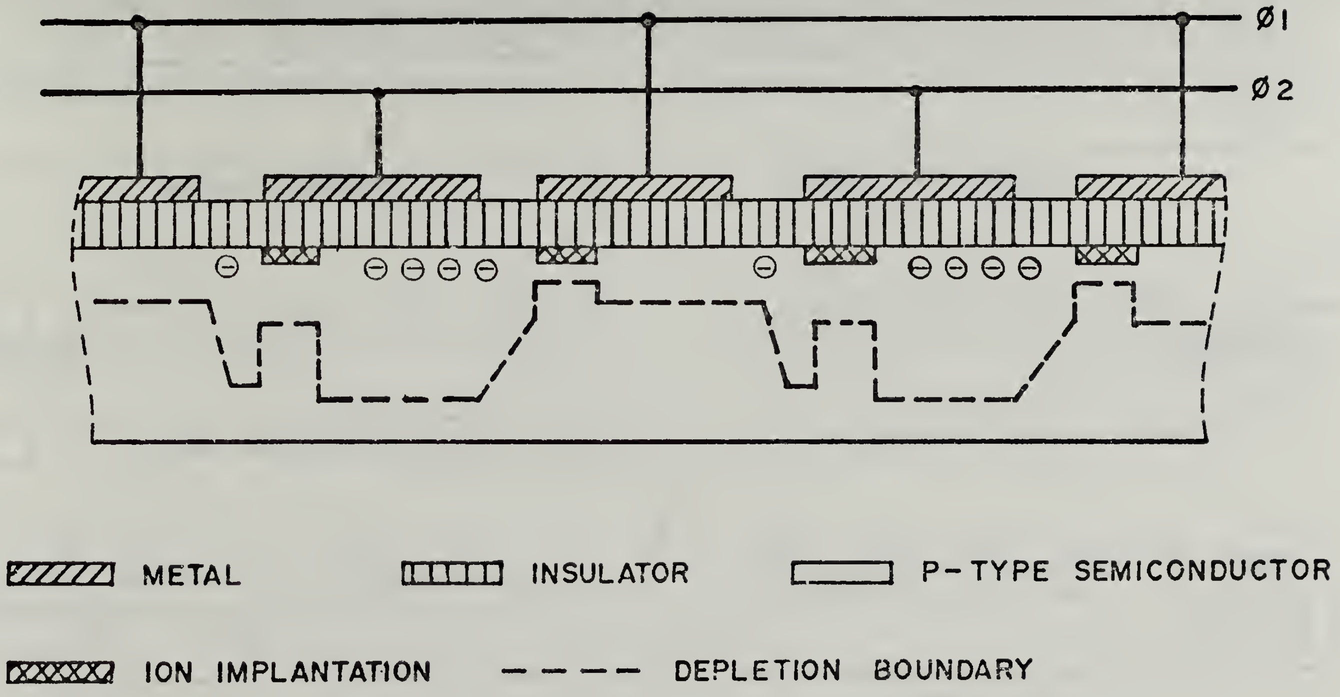
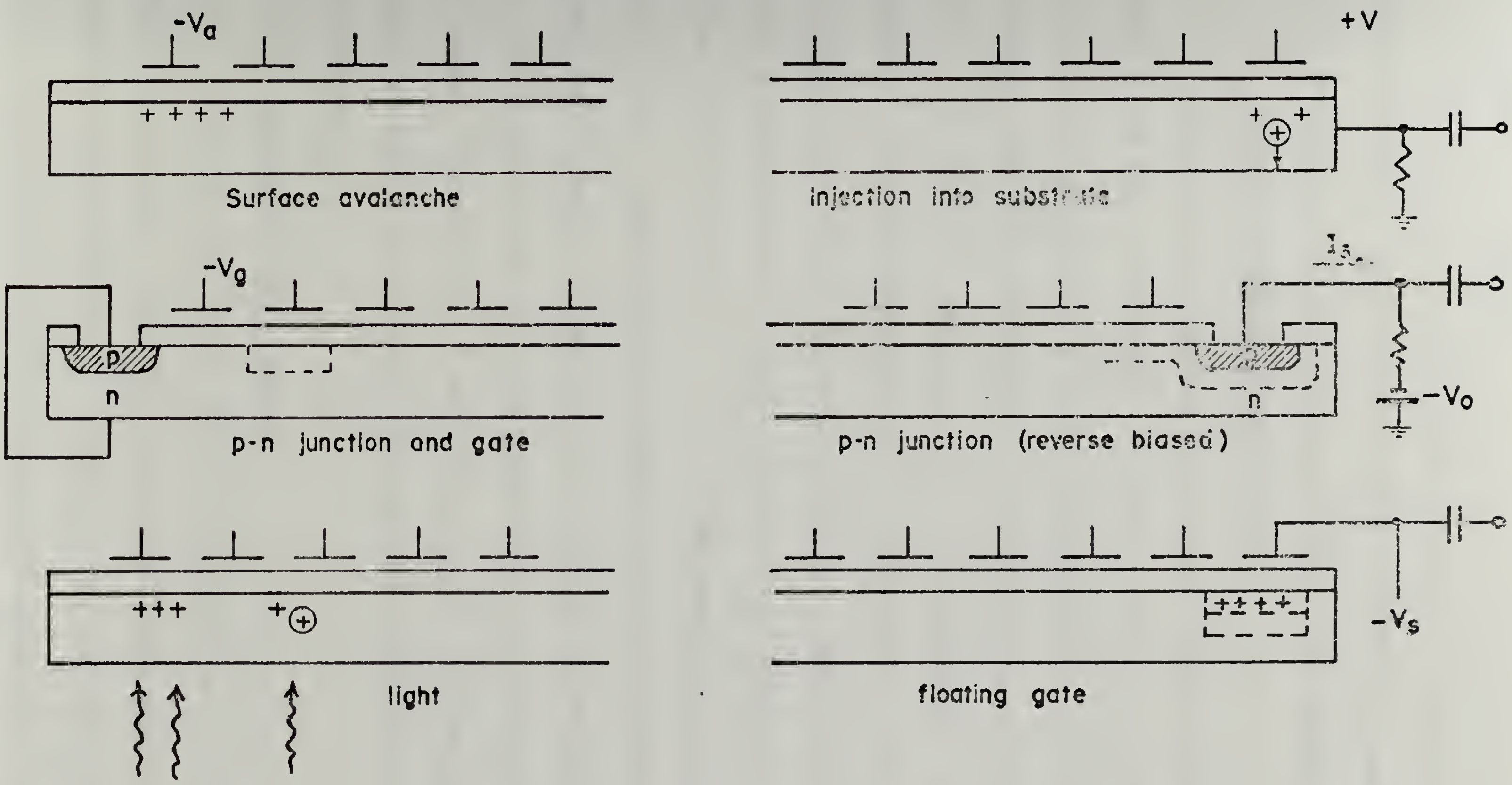

Ø1
Ø2
METAL
INSULATOR
P-TYPE SEMICONDUCTOR
ION IMPLANTATION
DEPLETION BOUNDARY

Figure 2-2. Construction and Operation of an Ion Implantation 2ϕ-CCD


-Va
+ + + +
Surface avalanche
-Vg
p
n
p-n junction and gate
+++
light
+V
injection into substrate
-Vo
n
p-n junction (reverse biased)
-Vs
floating gate

(a) Input Schemes

(b) Output Schemes

Figure 2-3. Input and Output Schemes of a CCD

D. FIGURES OF MERIT

Several figures of merit have been defined: quantity of stored charge, efficiency of the transfer, equilibrium time after deep depletion (storage time) and charge conservation.

1. Charge Storage Capability

This is the ability of the CCD to store charge. It depends on the following factors: energy gap, doping and dielectric constant of the semiconductor, the dielectric constant and the thickness of insulator, and the interface states of the MIS structures. A measure of charge storage capacity is the capacitance of the device which can be obtained from the C-V relationship. The stored charge is divided between the insulator and the depletion capacitance in the semiconductor. It is, of course, beneficial to have most of the charge in the semiconductor, however, there is a maximum charge at which the surface potential of a cell has the same value as its adjacent cells and the device can no longer function. A useful plot in estimating maximum charge ability is a plot of surface potential vs applied gate voltage.

2. Transfer Efficiency

One of the most important figures of merit is the amount of charge transferred or the transfer efficiency, η. Often the efficiency, or lack of it, is described in terms of the percentage of charge remaining after a transfer. The efficiency can be discussed in terms of element efficiency per transfer or device efficiency and values up to 99.995%

are common [26]. The importance of this figure of merit is amply demonstrated in the various reports on the worth of CCD's where the transfer efficiency is the prime interest [3, 7, 17, 27]. A measure of the difference between the amount of charge that exits a CCD to the charge input by any means is given by η. The cause of this loss is of major concern.

One of the major sources of charge loss are the interface states. These states are energy levels within the energy gap of the material that fill up rapidly but empty more slowly and as a result some travel with the charge packet from whence they came and others join up with a following packet. The study of interface state density in $Pb_{1-X}Sn_XTe(Se)$ alloy semiconductor MIS samples is of major interest in this thesis project. Two ways to eliminate this detrimental effect is to fill the interface states with background charge (the so-called fat zero approach) or move the interface deeper into the semiconductor (the so-called buried channel approach).

3. Transfer Time, t_0

The transfer time, defined by the time necessary for charge transfer to an adjacent cell, is due primarily to diffusion but is aided significantly by parallel interelectrode electric fields existing in the device. The transfer time should be shorter than the thermal diffusion time for minority carriers.

4. Storage Time, t_s

The storage time is defined as the time for a pulsed CCD element to return to the steady state conditions. It is a function of device capacitance, applied voltage, and the dark current of the device.

Storage time is an important parameter since it determines the lower limit of the operating clock frequency of the device. Storage time must necessarily be longer than the period of the clock frequency or the device will not function properly. This thesis project will also consider storage time which can be measured in principle. Typical values are $t_s \geq 0.5$ sec for Si-MOS-CCD and for imaging applications t_s must be much greater than the optical integration time. Storage times are affected by surface states whose energies lie within the energy gap of the semiconductor. Surface states consist of layer states characteristic of the oxide and interface states. Of the various types of layer states, interface states (of lower density) are more significant since they have a higher minority carrier capture cross section.

5. Charge Conservation

Charge can be lost or gained in the interelectrode gap region. If the region between electrodes is allowed to enter accumulation, and there are minority carrier traps present, recombination and trapping will occur and minority carriers are pumped into the substate and lost. To prevent this loss, one must ensure that the interelectrode gap

regions are depleted. The reverse may occur if minority carriers from the substrate move into the charge packet at the edge regions of the gate electrodes. This effect is small if channel-stop regions are used.

E. NON-INSULATOR CCD

The surface states are a real concern in CCD's and a possible way to eliminate this adverse effect is to provide a buried channel in which the minority carrier charge can form and move. The buried channel essentially eliminates the surface state trapping effect. A uniquely different buried-channel CCD which has no oxide interfaces has recently been proposed [22]. This section is presented separately for reasons which will be evident later. These reasons are the result of evaporating a form of alumina which had characteristics of a conductor and not an insulator.

The two proposed CCD's are the double-junction CCD (DJCCD) and the Schottky-barrier CCD (SBCCD); both CCD's are void of an insulation layer, characteristic of CCD's. The DJCCD is a p^+-n-p^- structure for n-channel CCD and the potential well is formed between two reverse biased pn junctions. Figure 2-4 gives the conduction band profile of the device. Curve A in the figure applies for 0V on the gate, B for +2V and C for -2V. The potential well is clearly formed in the n-type region and, as can be seen from the figure, more that 90% of the potential applied to the device goes into providing the depth of the potential well. This

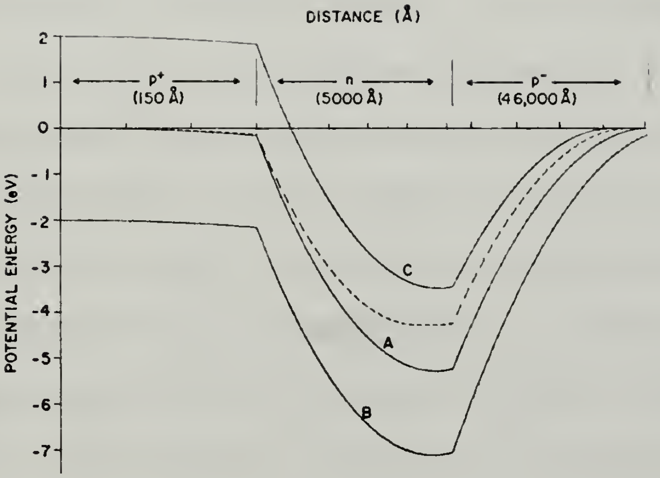


Figure 2-4. Theoretical Conduction-Band Profile for a Double-Junction CCD

effect allows for excellent efficiencies as far as charge capacity is concerned.

The SBCCD is basically similar to the DJCCD. However, the p^+ region is replaced by a metal layer. Its charactertics are similar to the DJCCD except that leakage current is larger.

These devices are very promising because of various reasons, the most important reason is the elimination of the interface states with the removal of the insulator layer. This reason is a distinct advantage to the laboratory that can produce good semiconductors but bad insulators. A second real advantage for the DJCCD is the fact that the clock driving voltage can be positive, negative or sinusoidal since the depletion region is produced by varying the dc bias on the gate and not on the clock pulse. A third advantage is that these devices are not so vulnerable to radiation as standard MIS CCD's are since the radiation affects the insulator greatly and the insulator has been eliminated.

The feasibility of producing such devices in the Naval Postgraduate Solid State Laboratory is somewhat promising since good semiconductor deposition, on Pb-Sn-Te(Se) alloys has progressed to a fine art. On completion of the multisource deposition scheme, the laboratory will have the capability to produce such devices on a daily basis. Heterojunctions have already been produced for application to heterojunction lasers [10].

III. REVIEW OF MIS CHARACTERISTICS

The basic characteristics of the CCD are determined by studying the MIS.[3] Three major parameters determined are the surface potential, ϕ_S, as a function of applied voltage, the storage time, and the surface state density. The surface state density affects the transfer efficiency, the storage time puts a lower limit on the clock frequency of the CCD and ϕ_S is an indication of the depletion width which is related to the amount of charge stored. This chapter first reviews the basic properties of the MIS and the methods of their investigations such as the capacitance-voltage (C-V) curves, the conductance-voltage (G-V) curves, the capacitance-time (C-T) curves and the derivatives of the C-V and G-V curves. This discussion pertains both to the ideal MIS which contains no interface states (N_{SS}), no metal-to-semiconductor work function difference (ϕ_{MS}), negligible bulk semiconductor and insulator resistance, and the non-ideal case where these parameters are considered.

A. DESCRIPTION OF AN IDEAL MIS

In this section the basic MIS structures are discussed. It is important to note that no new theory was developed in

---

[3] The MIS structure is the basic cell of a CCD whereas the basic element of a CCD is a set of 2, 3 or 4 cells (MIS) depending on the clock pulse scheme used.

this thesis but, rather, MIS structures of lead-tin alloys were analyzed following the existing theory developed for silicon MIS devices.

Figure 3-1 provides a diagram of the energy bands and charge distribution in an ideal MIS for the accumulation, depletion and inversion conditions in a p-type semiconductor. The development here will deal mostly with p-type devices since p-type lead-tin alloy semiconductors were in abundant supply to be tested whereas the supply of n-type devices was limited.[4]

In a p-type MIS, when a negative bias[5] (positive bias for a n-type MIS) is applied to the gate, the majority carriers (holes) are attracted to the interface between the semiconductor and insulator by the attractive forces of the net negative charge on the gate. Accumulation is depicted in part a. of Fig. 3-1 with the bands bending upward. With no bias applied, a flat-band condition exists in which the energy bands are flat. When a small positive bias is applied to the gate, majority carriers are pushed away from the surface and a depletion region is formed. This is shown in part b. of Fig. 3-1 and the bands are bent

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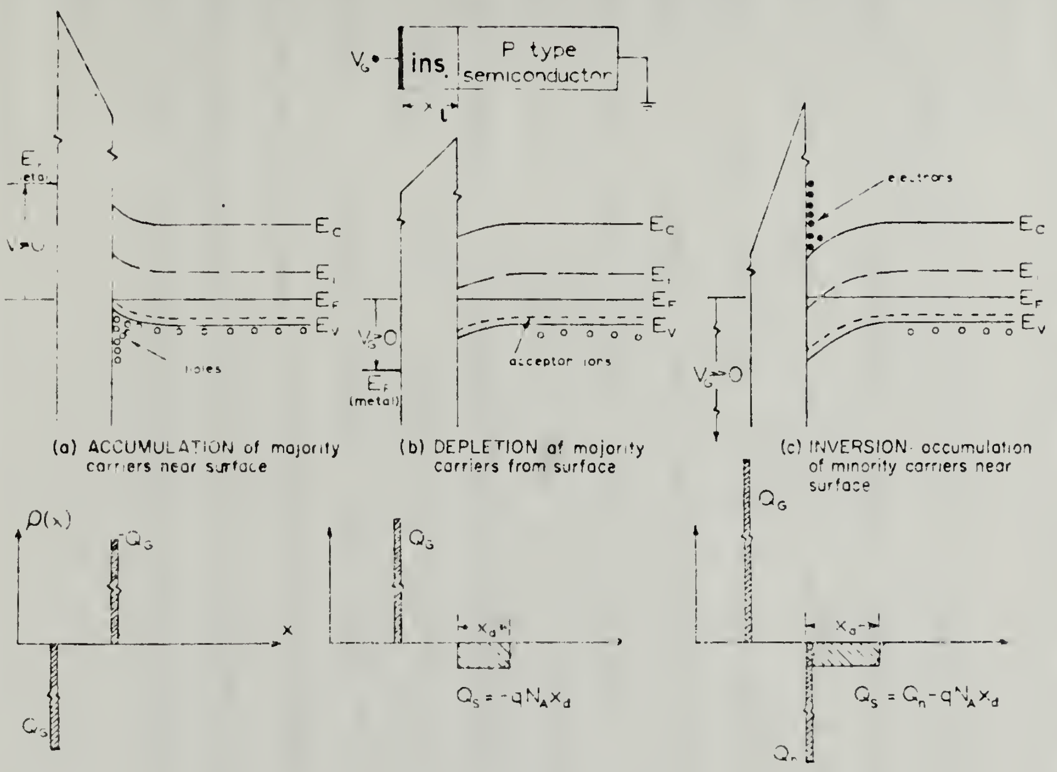
[4] The prepared n-type sample concentrations were in the mid 10^{19} range and showed no C-V variation.

[5] The bias on a MIS will always be with reference to the substrate.


(a) ACCUMULATION of majority carriers near surface

(b) DEPLETION of majority carriers from surface

(c) INVERSION: accumulation of minority carriers near surface

V_G
ins.
P type semiconductor
x_i
E_F (metal)
$V_G < 0$
$V_G > 0$
$V_G \gg 0$
E_C
E_i
E_F
E_V
holes
acceptor ions
electrons
$\rho(x)$
$-Q_G$
Q_G
x
x_d
$Q_s = -qN_A x_d$
$Q_s = Q_n - qN_A x_d$
Q_n

Figure 3-1. Energy Bands and Charge Distribution in Ideal MIS for Various Bias Conditions

downward.[6] If the positive bias is increased further, minority carriers (electrons) will be attracted to the interface and form an inversion layer. As the positive bias becomes even larger, more and more minority carriers will exist in the inversion layer. In the latter two cases the energy bands are bent down further as shown in part c. of Figure 3-1.

It is important to note that the above description, in the depletion and inversion region, applies only if the bias change is slow enough for minority carrier formation at the interface. This condition is the dc or low-frequency case in which it is assumed that the minority carriers are generated and moved to the surface and that the majority carriers (holes) formed in the rest of the depletion region are removed. The minority carrier charge formation may not always occur. Whether it does or not is of major importance to CCD applications since the rate at which the inversion layer appears determines the storage time. In the development which follows it is assumed that the dc bias is varied slowly enough for the minority carriers to follow.[7]

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[6] The intrinsic condition occurs when an equal number of minority and majority carriers exist at the surface. The mid-gap energy level at the surface, in this case, is equal to the Fermi band, and the corresponding bias voltage is referred to as the threshold voltage.

[7] This concern does not apply to the majority carriers whose relaxation time constant is very short, $t = \varepsilon/\sigma$.

An expanded view of the energy band diagram of a p-type MIS under inversion condition is shown in Fig. 3-2. The parameters used in Figure 3-2 are:

E_V = valence band level

E_C = conductor band level

E_i = intrinsic band level

E_F = Fermi level in semiconductor

E_{FM} = Fermi level in metal

ϕ_{SC} = work function in semiconductor

ϕ_M = work function in metal

ϕ = potential in semiconductor

ϕ_b = potential in semiconductor bulk

ϕ_s = potential at semiconductor surface

In the ideal case, the space charge within the semiconductor is given by

$$Q_s = \int_{X=0}^{\infty} \rho(X)dX \qquad (1)$$

where $\rho(X) = q(p-n + N_D - N_A)$, X = 0 is at the interface, ρ and n are the carrier concentrations and $N_D - N_A$ is the impurity concentration. For nondegenerate semiconductors in thermal equilibrium, Eq. 1 can be solved by applying Poisson's equation and Gauss' law in the space charge region [4]. The solution is

$$Q_s = -2 \frac{u_s}{|u_s|} qn_i L_D \left\{ 2 (\cosh (u_s-u_b) -\cosh u_b + u_s \sinh u_b) \right\}^{\frac{1}{2}} \qquad (2)$$

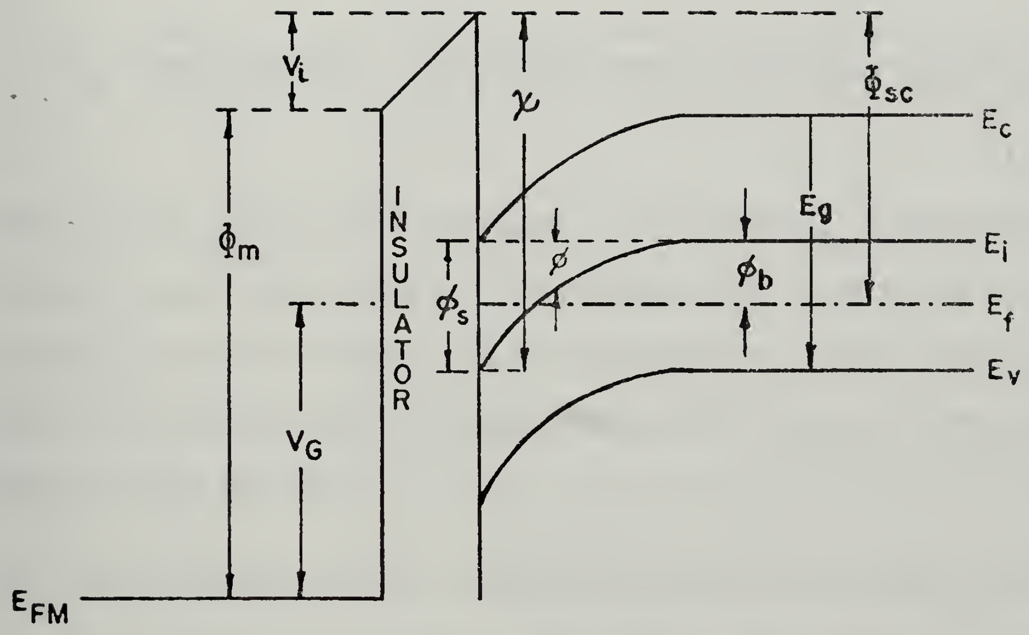
V_i
χ
Φ_{sc}
E_c
Φ_m
INSULATOR
E_g
E_i
ϕ
ϕ_s
ϕ_b
E_f
E_v
V_G
E_{FM}

Figure 3-2. Expanded View of MIS Energy Band Diagram Under Inversion Conditions

where L_D is the Debye length given by

$$L_D = \left[\frac{kT}{q}\,\frac{k_S\ \varepsilon_0}{2qn_i}\right]^{\frac{1}{2}} \tag{3}$$

and $u_{s(b)}$, in kT/q units, is the potential at the surface (in the bulk) of the semiconductor. Q_n, which is the inversion layer contribution to Q_s, is given by

$$Q_n = \frac{-u_s}{|u_s|}\, qn_i L_D \int_{u_b}^{u_s} \left\{ \frac{\exp\,(u - u_b)\, du}{2[\cosh(u-u_b) - \cosh u_b + u \sinh u_b]^{\frac{1}{2}}} \right\} . \tag{4}$$

These quantities are important since from Q_S the space charge capacitance can be determined and from Q_n the charge in the inversion layer can be determined. The latter quantity is instrumental in describing the charge storage capacity of the device.

B. CAPACITANCE-VOLTAGE CHARACTERISTICS OF AN IDEAL MIS

One of the best known and widely used tools to study the nature of the MIS is the capacitance-voltage (C-V) curves. Shown in Fig. 3-3 is an ideal C-V curve for a p-type MIS. Notice from the figure that the vertical scale contains capacitance normalized to the insulator capacitance (C_i).

1. Description of Typical C-V Curves

The information in a C-V plot is contained in the depletion and inversion regions of the capacitance plots. In the accumulation region the maximum capacitance the MIS

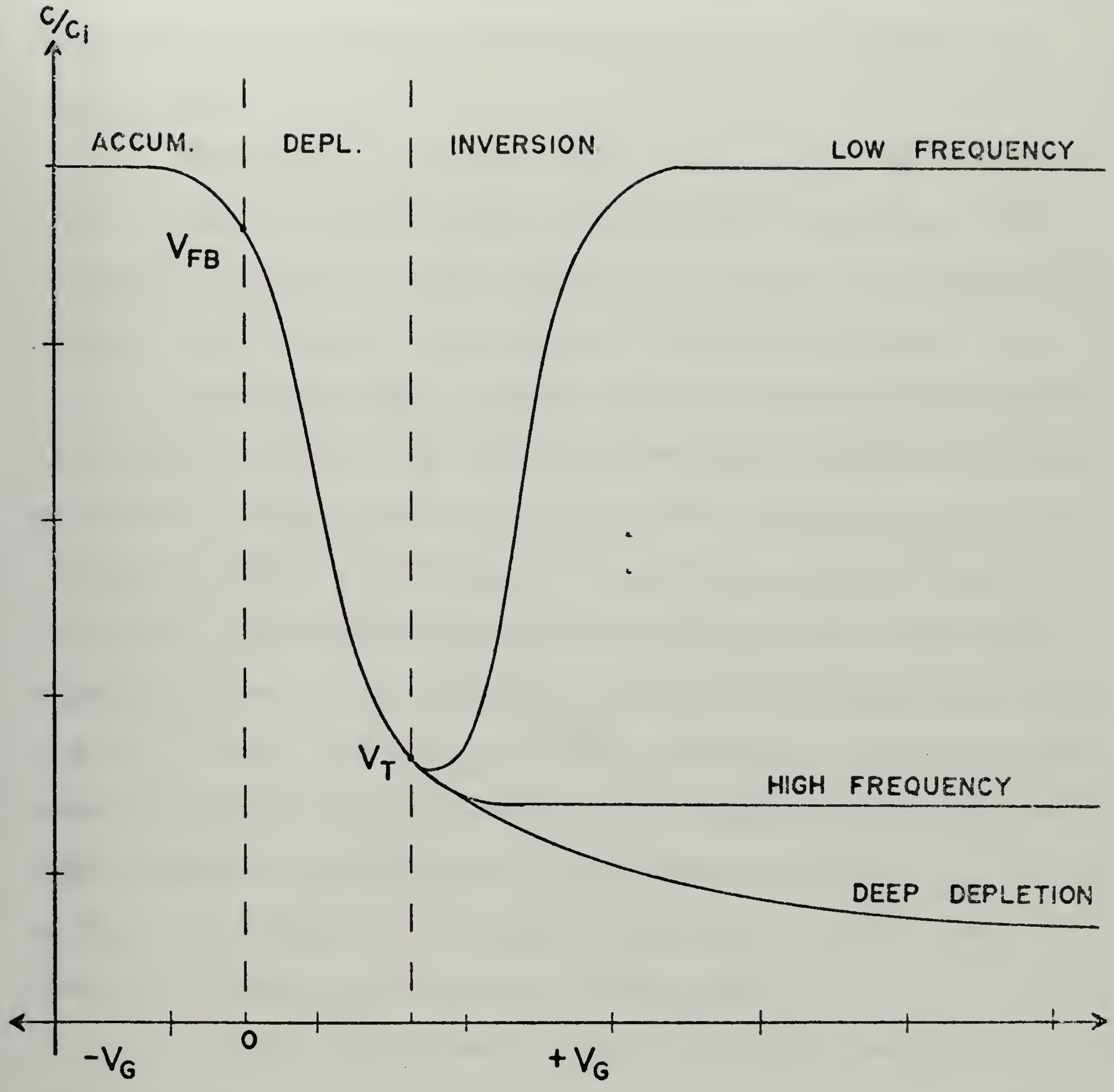

Figure 3-3. Ideal C-V Curves for p-Type MIS

device can have is the insulator capacitance. The insulator capacitance shields any detectable change in surface capacitance.

The capacitance in a MIS structure can be divided into 5 types. These are the accumulation, depletion, low-frequency inversion, high-frequency inversion, and high-frequency deep depletion capacitances (depicted in Fig. 3-3).

The first three types of capacitance were described in section A above. In the high-frequency inversion case the ac signal frequency is so high that the change of inversion charge (increase and decrease of minority carriers due to ac signal) can not be supplied by the generation and recombination rates in the semiconductor and the capacitance levels off. This condition is really a partial inversion case where the minority carriers act like fixed charges and the semiconductor capacitance is effectively given by $C_{inv} = \varepsilon_s/X_{inv}$ and exists for surface potentials greater than about two times the potential in the bulk.

In the high-frequency deep depletion case the dc bias sweep and ac signal are both rapid enough not to allow the inversion charge to form. As a result, the capacitance value decreases even further from the inversion case and goes to zero, in theory.

2. Theoretical C-V Equations

In the low-frequency inversion case the total capacitance of the device is given by the series combination of the insulator capacitance and the space charge capacitance.

$C = \frac{C_i \; C_S}{C_i + C_S}$ which when normalized becomes:

$$\frac{C}{C_i} = \frac{1}{1 + C_i/C_S} \; . \qquad (5)$$

Since $C_S = - \frac{\partial Q_s}{\partial \phi_s}$, differentiation of Eq. 2 for Q_s above and substitution into Eq. 5 will yield the expression for the ideal low-frequency C-V value.

For the high-frequency inversion case, an effective depletion depth X_{eff} must be considered since the minority carriers do not follow the ac signal but are affected by it. The space charge capacitance per unit area is defined as

$$C_S = \frac{K_s \; \varepsilon_0}{X_{eff}} \text{ where } X_{eff} \text{ is } X_{eff} = \int_0^{u_s} \frac{1 - e^u}{F(u,u_b)} \, du \qquad (6)$$

and $F(u,u_b)$ is the term enclosed in brackets in Eq. 2. The high frequency capacitance then becomes Eq. 5 with Eq. 6 substituted for C_S.

In high-frequency deep depletion case, the C-V relationship is like that of a reverse biased p-n junction. This is really a transition case in which the MIS is not in equilibrium and can be caused by a leaky oxide or if the dc bias is rapidly swept from accumulation into inversion. The capacitance is again given by Eq. 5 with a different value for X_{eff} since in this case there is no inversion layer and $Q_s = q(N_D - N_A)X_{eff}$. The capacitance can be found to be [4]

$$\left(\frac{C}{C_i}\right)_{DD} = \frac{1}{\left(1 + \frac{2K_i^2 \varepsilon_0 V_G}{q(N_A - N_D)K_S X_i^2}\right)^{\frac{1}{2}}} \quad . \qquad (7)$$

The deep depletion capacitance value is important in describing the storage time of the MIS.

C. CAPACITANCE-TIME CHARACTERISTICS OF MIS

When a MIS structure is pulsed from accumulation into deep depletion, the semiconductor surface potential is large at the onset of depletion but relaxes to the quasi-equilibrium inversion value in a certain characteristic time, T. This time is dependent on the rate of minority carrier generation at the interface and the rate at which the majority carriers drift to the bulk region to neutralize the ionized acceptor atoms. This C-t response characterizes the diffusion length, the minority carrier lifetime, and the surface generation velocity of the device. Other important parameters derived from the C-t response are the storage time, T, and a measure of the maximum amount of charge that can be stored in a MIS under pulsed conditions.

The C-t response of a MIS exists because the minority carriers can not follow the ac signal (or the pulsed dc bias). Figure 3-4 shows the relationship between the C-t and C-V curves. After the MIS capacitor is pulsed into deep depletion, it relaxes to the quasi-equilibrium high-frequency inversion in time T. This relaxation is due to the appearance of minority carriers at the interface by five

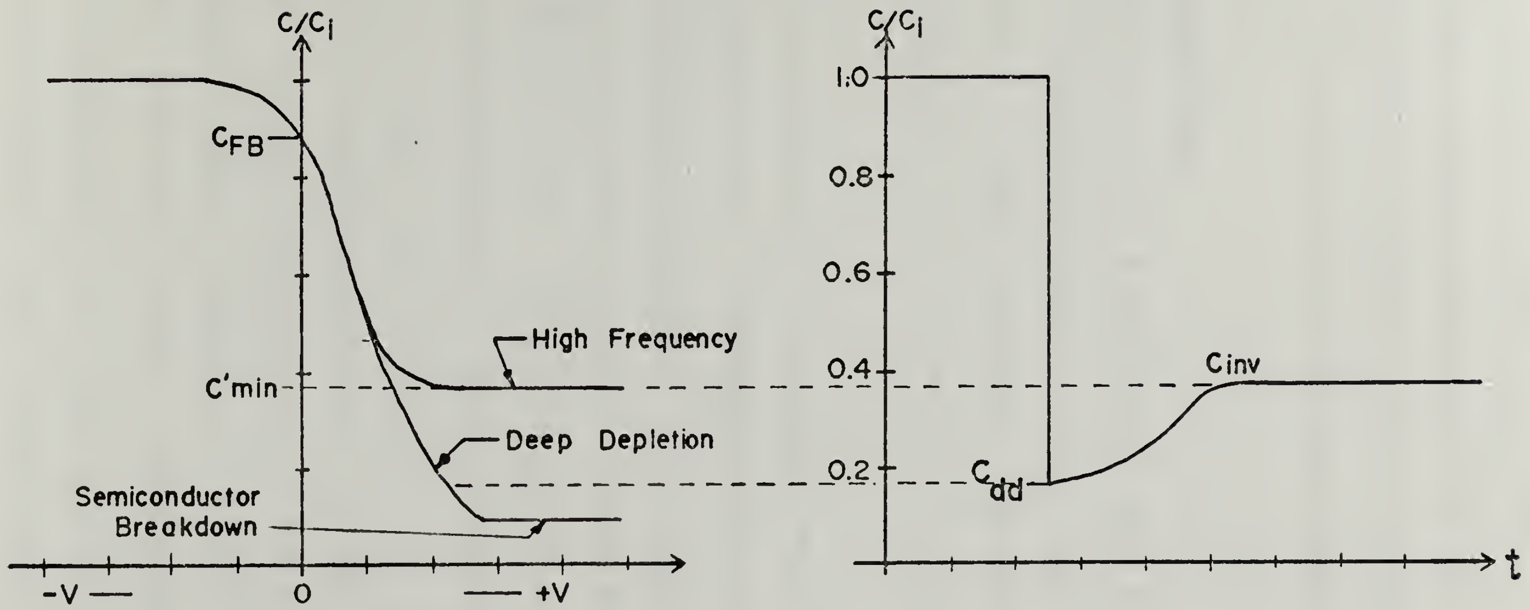

Figure 3-4. Accumulation to Inversion Pulsed Response of an MIS

possible generation mechanisms [21]: thermal generation in the depletion region, thermal generation in the semiconductor bulk region, thermal generation at the surface of the bulk, and external excitation such as photons and energetic electrons. The consequence of these mechanisms is discussed below.

1. Storage Time

The time, T, is a measure of MIS storage time which determines the maximum amount of time that a MIS, once pulsed, remains in deep depletion. In MIS-CCD applications this time determines or sets the lower limit on the clock frequency.

In the absence of an external source of minority carriers, storage time is controlled by the rate of thermal generation of minority carriers. In semiconductors, like the indirect gap silicon, this is a slow process and may take up to 200 seconds. Long storage times are favorable in CCD applications since it allows fewer unwanted non-signal carriers to enter into inversion. If the charge is dominated by the thermal generation in the depletion layer, this storage time is approximated by $T = 2\tau_0 N/n_i$ where τ_0 is the minority carrier lifetime, N is the impurity concentration, and n_i is the intrinsic carrier concentration. For practical CCD operation, the clock period of transfer should be at least one hundred times shorter than the storage time.

2. Storage Capacity

An important consideration for the CCD operation is the maximum amount of minority charge that can be stored in each MIS element. This maximum charge can be thought of as the amount of charge which when placed beneath the gate in the depletion region area of a MIS element in a CCD will raise the potential to that of its adjacent neighbor (to that of the surrounding area) i.e., the surface potential of the transfer element becomes that of the storage element.

In this thesis, the storage capacity is estimated by the following procedure. First, the theoretical C-V high-frequency inversion and high-frequency deep depletion capacitance-voltage curves are computed. Q storage is estimated as $Q_{store} = (C_{inv} - C_{DD})\, V_{inv}$ where V_{inv} is the gate voltage in the inversion region.[8]

D. OTHER RELATED MIS CHARACTERISTICS

Other methods used to investigate a MIS structure are the conductance-voltage (G-V) curves and the derivatives of both the C-V and G-V curves. The G-V curves are not as popular as C-V curves in describing a MIS because not as much information can be obtained from these curves as can be obtained from the C-V curves. For instance, the dC/dV curve's peak is a good indication of the flat-band voltage and G-V curves allow the determination of interface state

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[8] An example of the output obtained from the computer program output appears in Chapter VIII.

density. The information obtainable from the C-V curve are carrier concentration, surface potential versus applied voltage, and interface states among others. The dC/dV curve is similar in appearance to the G-V curve in that both have peaks in the depletion region and are flat in accumulation and inversion. The experimental determination of these curves was not attempted in this thesis.

E. C-V CHARACTERISTICS IN REAL MIS

The shape of the ideal C-V curve, shown in section B, above, pertains to a structure with no insulator charge, no work-function difference between metal and semiconductor, no interface states, and no surface charge. Flat-band condition (i.e., where the surface potential goes to zero) is also zero in this case. In this section the characteristics of a real MIS are discussed.

1. Physical Changes

In Fig. 3-5 the changes in the real insulator which made it different from the ideal case are shown. A first change is the insulator charges which could include the fixed insulator charges, ionized traps, mobile ions and interface states. Second is the interface states in the semiconductor. Third is the work function difference.

The insulator charge has the effect of producing a change in the potential of the semiconductor. This effect was deliberately introduced in the oxide insulator of silicon nitride in the uniphase CCD described in Chapter II, to produce potential wells in the semiconductor for directional

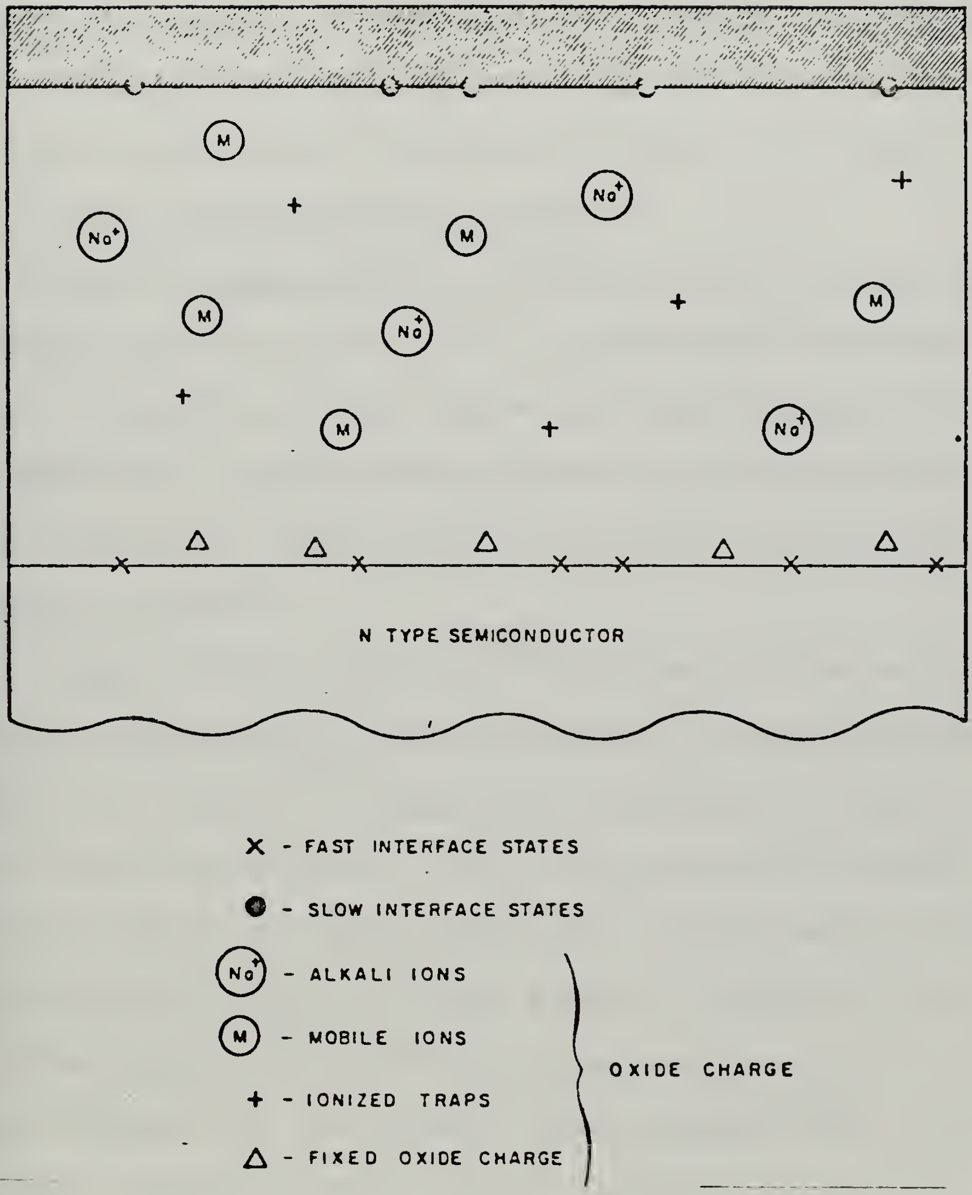
M
Na+
N TYPE SEMICONDUCTOR
X - FAST INTERFACE STATES
● - SLOW INTERFACE STATES
Na+ - ALKALI IONS
M - MOBILE IONS
+ - IONIZED TRAPS
△ - FIXED OXIDE CHARGE
OXIDE CHARGE

Figure 3-5. Classification of Charges and States in a Non-Ideal MIS

charge packet flow. The interface states within the forbidden gap of the insulator and semiconductor ("traps") are occupied and emptied at different rates. Fast interface states react quickly and are usually found at the semiconductor-insulator interface whereas the slow states react slowly and are found at the metal-insulator interface.

2. Device Characteristic Changes

These changes refer to changes in the device characteristics such as the C-V, G-V, C-t and their derivative curves. In addition to the above mentioned causes of non-ideal behavior, the following factors also effect these curves. These are high contact resistance and high bulk generation lifetime.

When the only departure from ideal is the work function difference ϕ_{ms}, the C-V curve is simply shifted parallel to the left or right and the amount of shift is equal to this difference.[9] When the departure includes interface states that are independent of the swept dc bia , then the curve is also a simple parallel shift on the voltage axis. The amount of interface states is a measure of the charge occupancy of the states. The voltage shift including these two effects is $\Delta V_G = \phi_{MS} - Q_{SS}/C_i$.

When the interface states become dependent on the applied dc bias, whose density varies within the energy gap,

---

[9] The shift is to the left for negative ϕ_{MS} and to the right for positive ϕ_{MS}.

the curve is shifted in a non-parallel fashion along the voltage axis but the ratio of maximum to minimum capacitance is unchanged from the ideal case. In the most extreme case where the surface states do not follow both the ac signal and dc bias, the maximum amount of deviation from the ideal case exists. Figure 3-6 provides a family of curves showing the effect of the non-ideal parameters described above. These curves can be considered a "finger print" of non-ideal curves and as such can be used to rapidly evaluate the quality of a MIS structure after an experimental curve is obtained. Note from the figure that part a. is simply the deep depletion case described in section B.

Also displayed in Fig. 3-6 is the hysteresis[10] effect present in some MIS samples. The amount of hysteresis in C-V curves is determined by the amount of current passing into and through the insulating film and by the amount of charge that is trapped in the insulator. Device hysteresis does not necessarily make it useless. It is feasible to obtain a greater quantity of charge storage in devices displaying hysteresis.

Another non-ideal characteristic is drift or the inability to trace repetitively similar characteristic curves.

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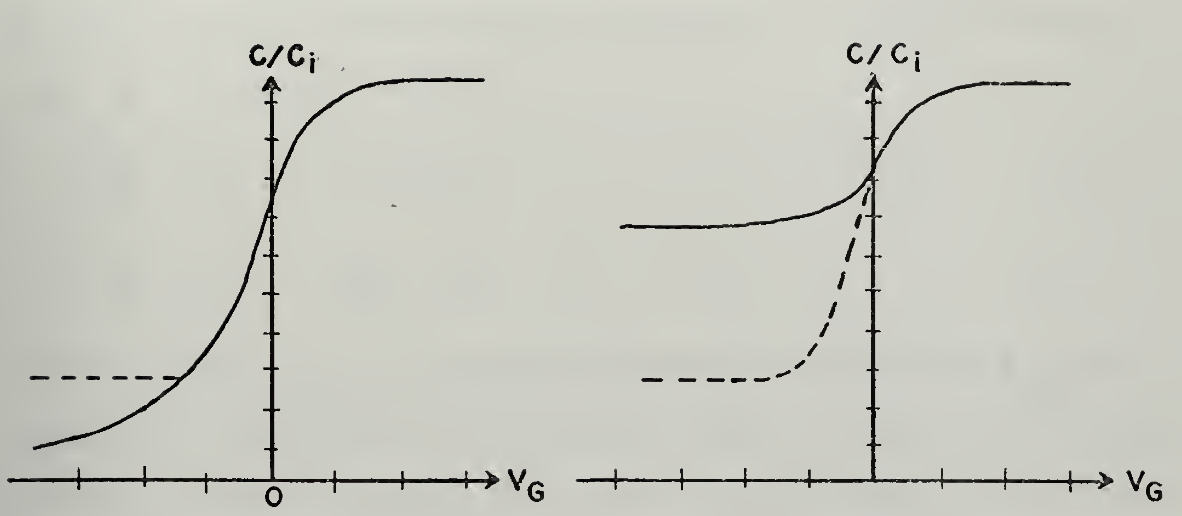
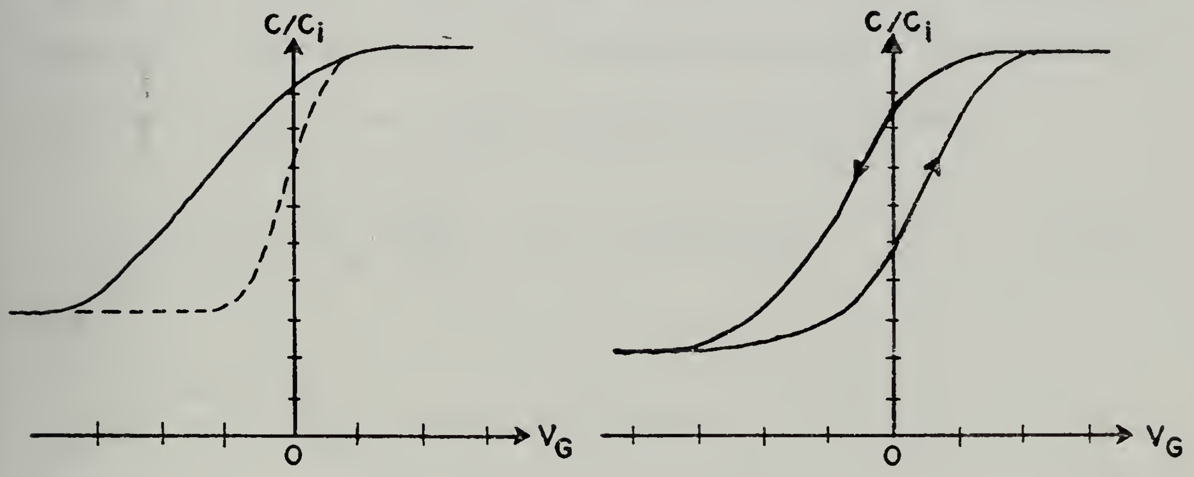
[10] Hysteresis is the inability of a particular MIS sample to characterize similar C-V curves when the device is biased from accumulation to inversion or from inversion to accumulation. Hysteresis also applies to G-V, I-V and the derivatives of C-V and G-V curves as well.



a) High Bulk Generation Lifetime

b) High Contact Resistance



c) Interface States

d) Hysteresis

Figure 3-6. "Finger Prints" of Non-Ideal MIS

3. Theoretical Changes

Two of the major non-ideal effects are the changes in the potential distribution in the MIS. They are signified in the Eqs. 8 and 9 .

$$V_a = V_i + V_S + \phi_{MS} \qquad (8)$$

$$-Q_M = Q_i + Q_{SS} + Q_S \qquad (9)$$

with the inclusion of the work function difference ϕ_{MS}, the insulator charge, and interfacial charge. Flat-band voltage is also changed and does not occur at $V_S = 0$ but is defined as $\phi_{MS} - Q_{SS}'/C_i$, where Q_{SS}' is the overall effect by the added charge. These changes can also be represented in the admittance of the MIS as shown in the equivalent circuit, Fig. 3-7. It can be obtained for experimental C and G measurements [28]. Their expressions are long and are not included in this thesis. The combined device capacitance in low-frequency and high-frequency cases become

$$C = \frac{C_i \, (C_S + C_{SS})}{C_i + C_S + C_{SS}} \quad \text{(low frequency)} \qquad (10)$$

and

$$C = \frac{C_i \, C_S}{C_i + C_S} \quad \text{(high frequency)} \quad . \qquad (11)$$

These two equations are used in the computer program to analyze the experimental data. Equation 11 was used above to calculate both the theoretical high and low-frequency capacitances with different values of C_S for each respectively.

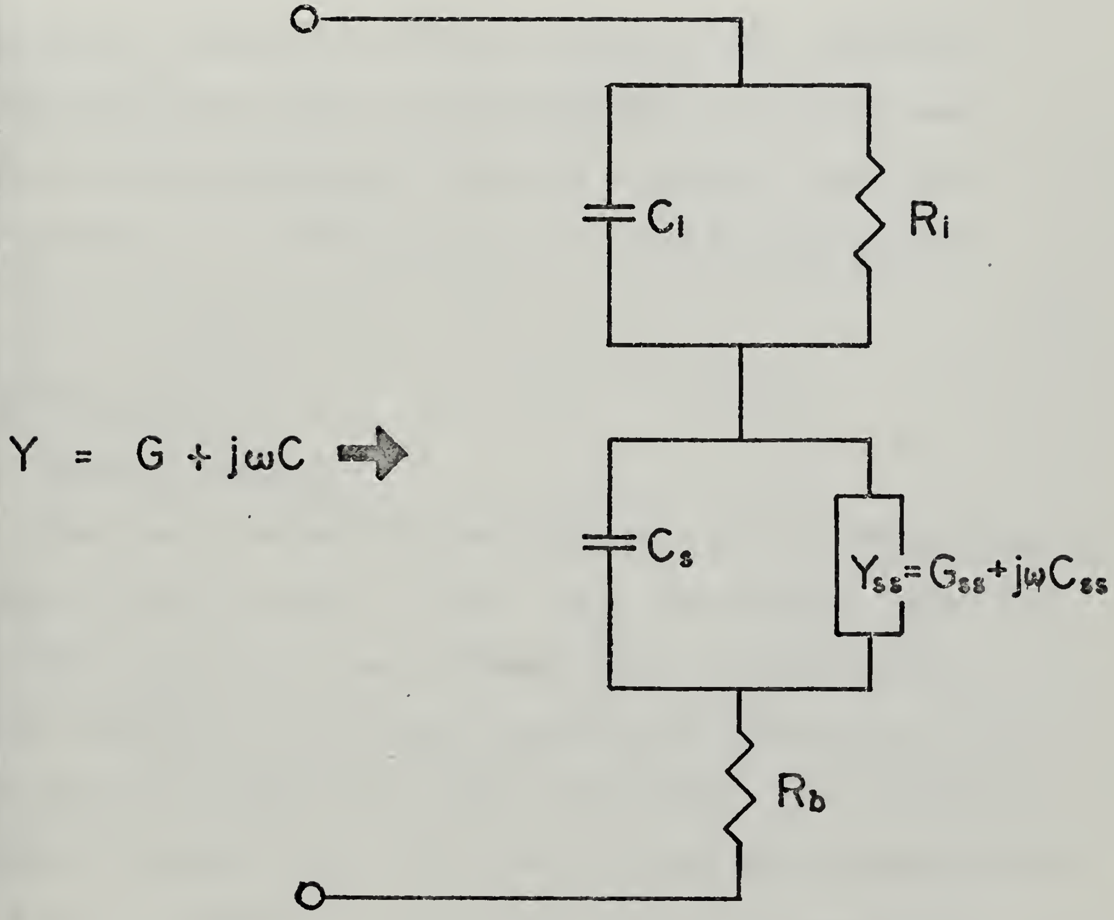

$Y = G + j\omega C$
C_i
R_i
C_s
$Y_{ss} = G_{ss} + j\omega C_{ss}$
R_b

Figure 3-7. MIS Equivalent Circuit

IV. MEASUREMENT TECHNIQUES ON MIS

The basic schematics of the equipment used and the problems associated with the experimental procedure are described in this chapter. Three measurements were used: high-frequency C-V, low-frequency C-V and high-frequency C-t.

A. HIGH-FREQUENCY C-V

1. Basic Schematic

The basic schematic for obtaining experimental high-frequency plots is shown in Fig. 4-1. The Boonton Model 72A capacitance meter provides a direct scale readout on X-Y recorder output for full-scale capacitance ranges of 1, 3, 10, 30, 100, 300, 1000, and 3000 picofarads. It requires a minimum of setup time. The bias voltage which ranges from ±200, ±400, or ±600Vdc is applied to the back terminals and automatically appears on the front test coaxial input connectors along with a 15 MV-1MHz ac signal.[11] The meter's phase sensitive detection system allows accurate capacitance measurement of devices with a Q as low as one. A dc output voltage which is proportional to the meter capacitance reading is available at output jacks for the input to an X-Y

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[11] The bias signal appears on the low-coaxial input connector if it is applied to the lo back jack input and vice versa.

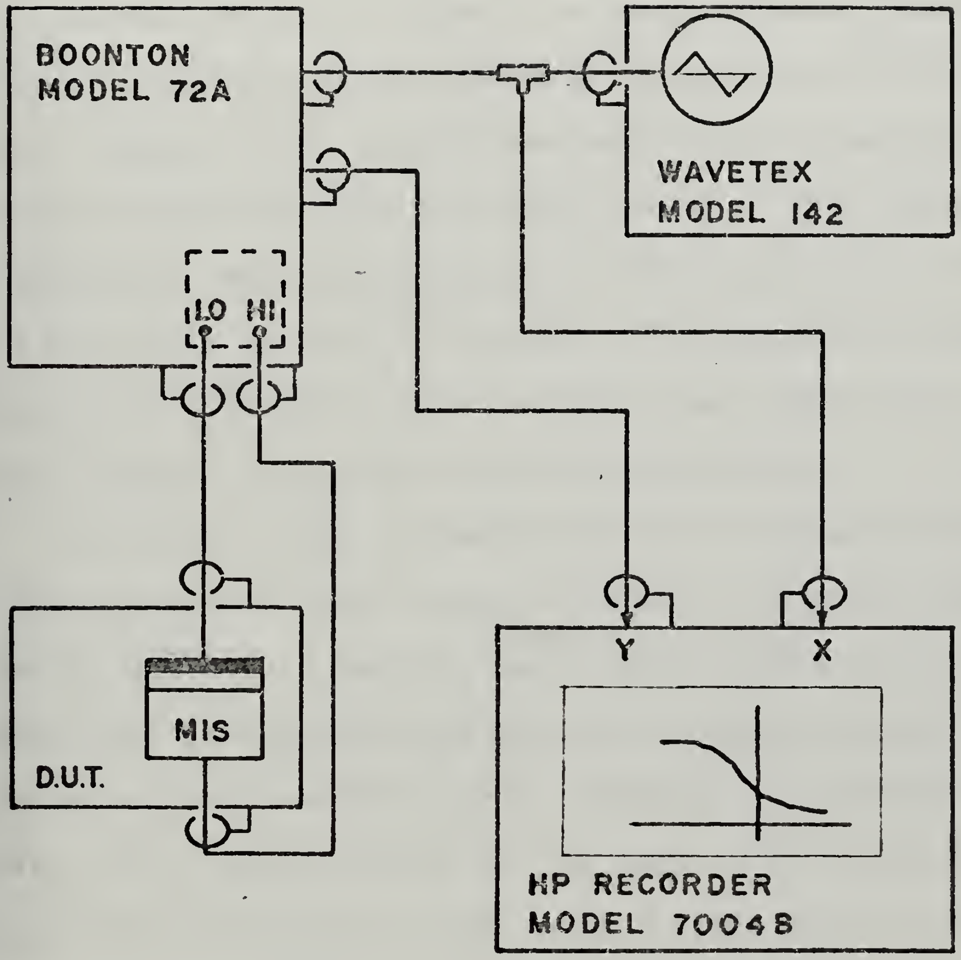
BOONTON
MODEL 72A
LO
HI
WAVETEX
MODEL 142
D.U.T.
MIS
Y
X
HP RECORDER
MODEL 7004B

Figure 4-1. Block Diagram for High-Frequency C-V, and C-t Measurements

recorder in terms of 1 or 3 maximum output voltage for the 1 and 3 series scale settings respectively.

2. Errors Due to Leaky Insulators

During the first phase of experimentation, difficulty was encountered with the measured capacitance of the lead-tin samples. The capacitance meter gave some readings on one scale but not at all on other scales. For example, the capacitance was 28 picofarads on the 30-p scale but overloaded the scale on the 100 p-scale. The cause of this difficulty was not due to the Boonton capacitance meter since it was pre- and post-tested for accuracy.

The first cause investigated was the possibility that the mechanical probe punched through the metal gate and the insulator. A second cause investigated was the possibility that the high electric field existing at the tip of the probe produced dielectric breakdown. To avoid these problems, soft indium solder on the probe tip was used. This prevented the high E field at the probe tip by spreading out the probe tip over a larger area. It did not eliminate the problem. When the mechanical probe tip was replaced by a small dot of liquid Hg, the problem among different scales was eliminated in some cases.

Further investigation showed that the dc leakage resistance of the insulator along the insulator surface and across it was approximately 1 KΩ. This check provided a rapid evaluation of the sample as to whether it would produce useful C-V curves. Only those samples whose

leakage resistance was greater than about 2KΩ gave useful curves.

In order to verify the effect produced by a leaky insulator, a shunt resistance box was placed across the MIS samples which were known to have a high value of dc resistance. Figure 4-2 and 4-3 show the effect produced for various values of shunt resistance. It is clear from the figures that shunt resistance (leaky insulators) produces a drastic change in the C-V curves of a MIS sample. In Fig. 4-2 the sample was a silicon MOS with insulator resistance of greater than 1 MΩ. In Fig. 4-3 the same effect as Fig. 4-2 was produced on a Ge-MIS which had an insulator resistance of 10 KΩ. It suggested that the C-V curves for a MIS with leaky insulators less than 1 KΩ resistance do not produce meaningful results. For leakage resistance between 1KΩ and 10KΩ, C-V curves are probably distorted. However, the changes in C-V depletion and inversion is still clearly evident.

B. C-t CURVES

1. Basic Schematic

C-t measurements were carried out using the same setup as for the C-V measurements. A square wave from the Wavetek signal generator was used. The voltage variation necessary to switch from accumulation to inversion was obtained from a check of the C-V curve which was accomplished prior to the C-t measurement. For those MIS whose storage

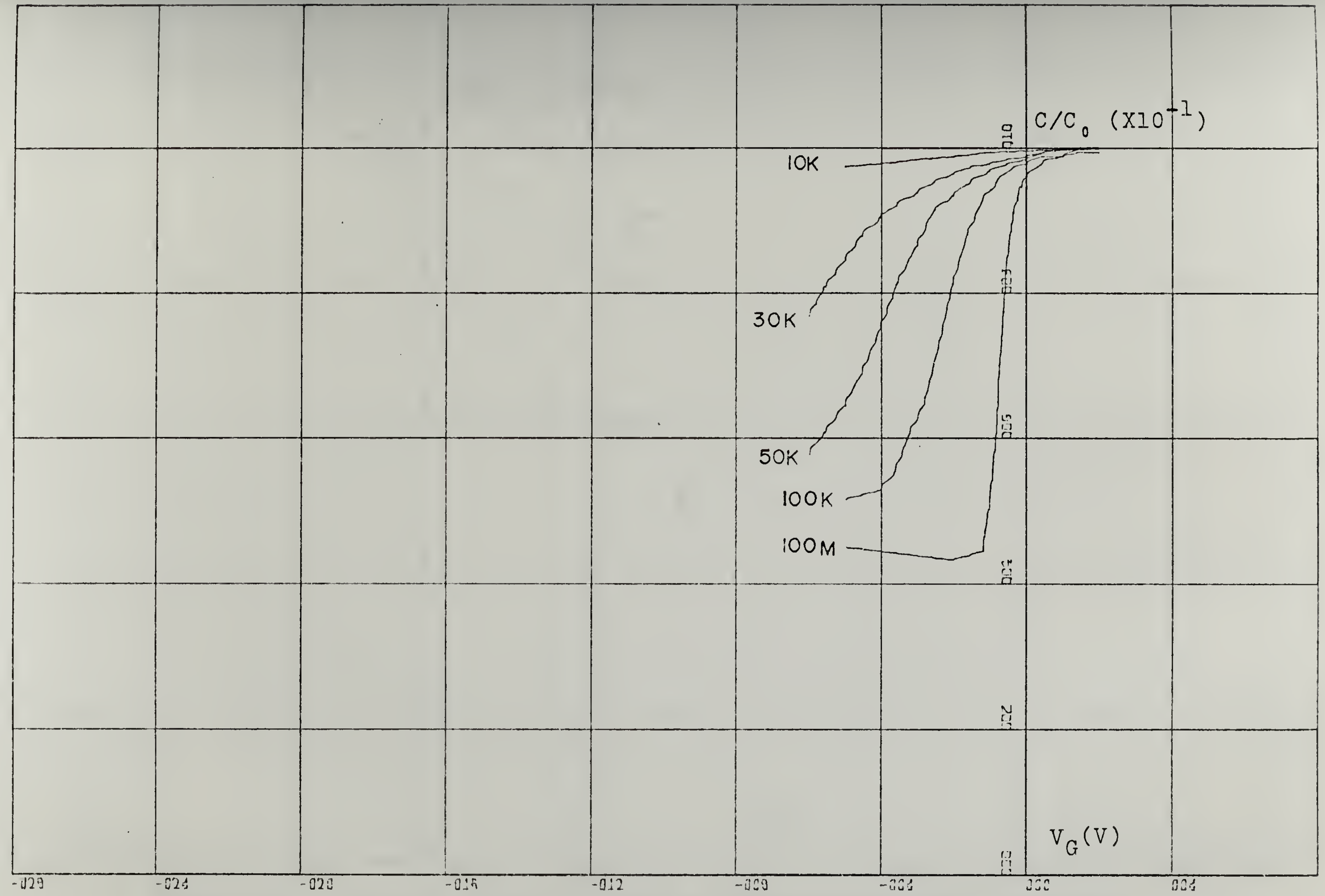

Figure 4-2. Leaky Insulator Effect on n-Type Si-MOS with Insulator Resistance Greater than 1MΩ

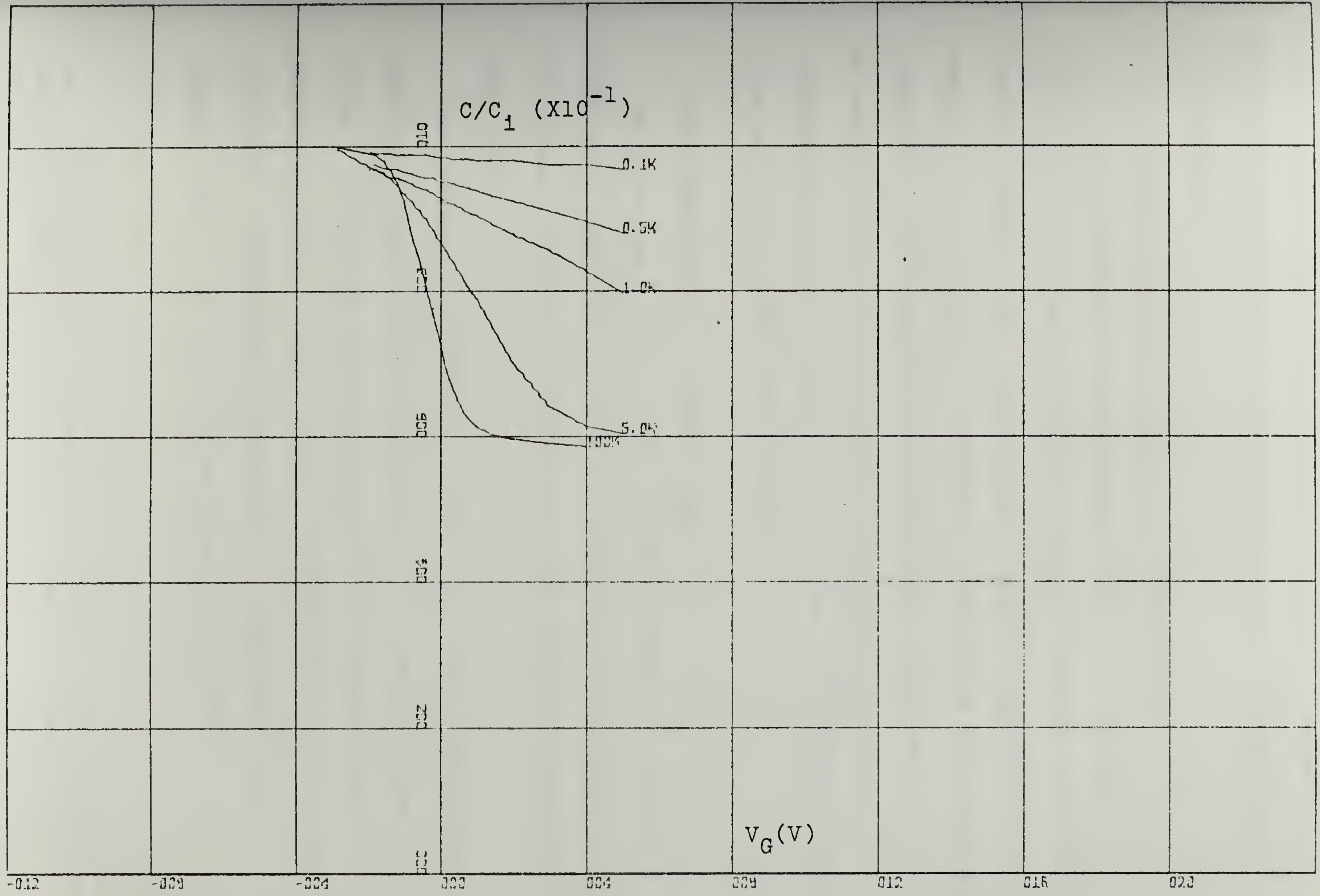

Figure 4-3. Leaky Insulator Effect on p-Type Ge-MIS with Insulator Resistance of 10KΩ

times are too short to be recorded on the X-Y recorder, a Tektronix Model 422 oscilloscope was used to observe the C-t response.

2. Errors Associated with C-t Measurements

C-t curves are unmeasurable when the insulator is leaky because of the available supply of minority carriers. For this reason, most lead-tin MIS samples displayed no C-t response. Moreover, C-t curves are observable only if a MIS displays a high-frequency deep depletion capacitance.[12] If no characteristic deep depletion capacitance is observed, the semiconductor is already in the quasi-equalibrium inversion and can not relax any further.

C. LOW-FREQUENCY C-V CURVES

Because the Boonton test frequency is set at 1 MHz, a different experimental setup is required for low-frequency C-V curves. The C-V experimental test setup is depicted in Fig. 4-4.

The Princeton Applied Research (PAR) Model 124 Lock-In-Amplifier (LIA) is the critical part in the experimental setup. A thorough understanding of how it functions is necessary before it can be used efficiently in obtaining meaningful experimental C-V curves. This section will consist only of a brief explanation of the LIA.

---

[12] High-frequency deep depletion capacitance depends on the sample type and also on the conditions under which the sample is measured, i.e., temperature and illumination conditions.

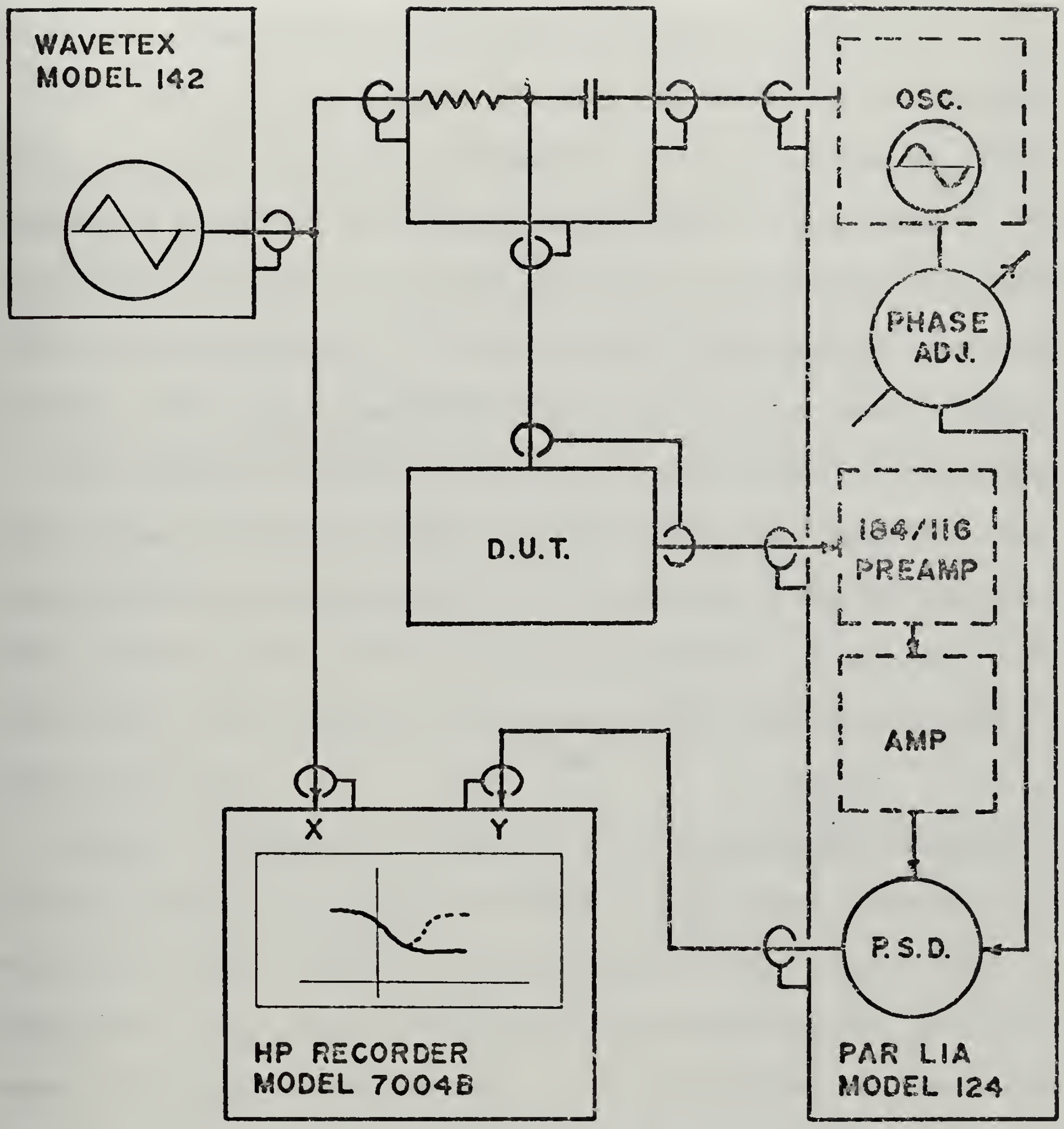
WAVETEX
MODEL 142
OSC.
PHASE
ADJ.
D.U.T.
184/116
PREAMP
AMP
X
Y
P.S.D.
HP RECORDER
MODEL 7004B
PAR LIA
MODEL 124

Figure 4-4. Block Diagram for Low-Frequency and G-V Measurements

Considerable information on its operation can be obtained from the various PAR application notes. [5, 25].

The LIA's forte is its ability to "lock-in" the signal frequency to the center frequency of the pass bands of the measuring circuits and tuned amplifiers in the device. This "lock-in" feature can be obtained for an external oscillator used as a reference or it may lock-in internally, depicted in Fig. 4-4, to an internally generated sine wave signal.

The signal detection ability extends down to the nanovolt range but at the high-sensitivity scale required for these nanovolt measurements, the noise problem is considerable. Fortunately the required sensitivity scale for C-V curves was high enough to eliminate the high sensitivity noise problems.

Signal detection in the LIA is accomplished through the use of a phase sensitive detector. The phase detector produces an output that is proportioned to the signal input amplitude, $/V_s/$, and the phase difference between the reference and signal input, $\phi_S-\phi_r$. The magnitude of the reference phase is not considered in the measurement.

Figure 4-5 shows the equivalent circuit which describes the low-frequency phase sensitivity measurements, $\tilde{V}$, $\tilde{V}_u$, $\tilde{V}_R$ and $\tilde{V}_S$ are the phasor quantities of the voltages at the various positions shown. When these four voltages are combined with the Thevenin equivalent voltage of the oscillator output as seen from the gate of the MIS, the following equation results

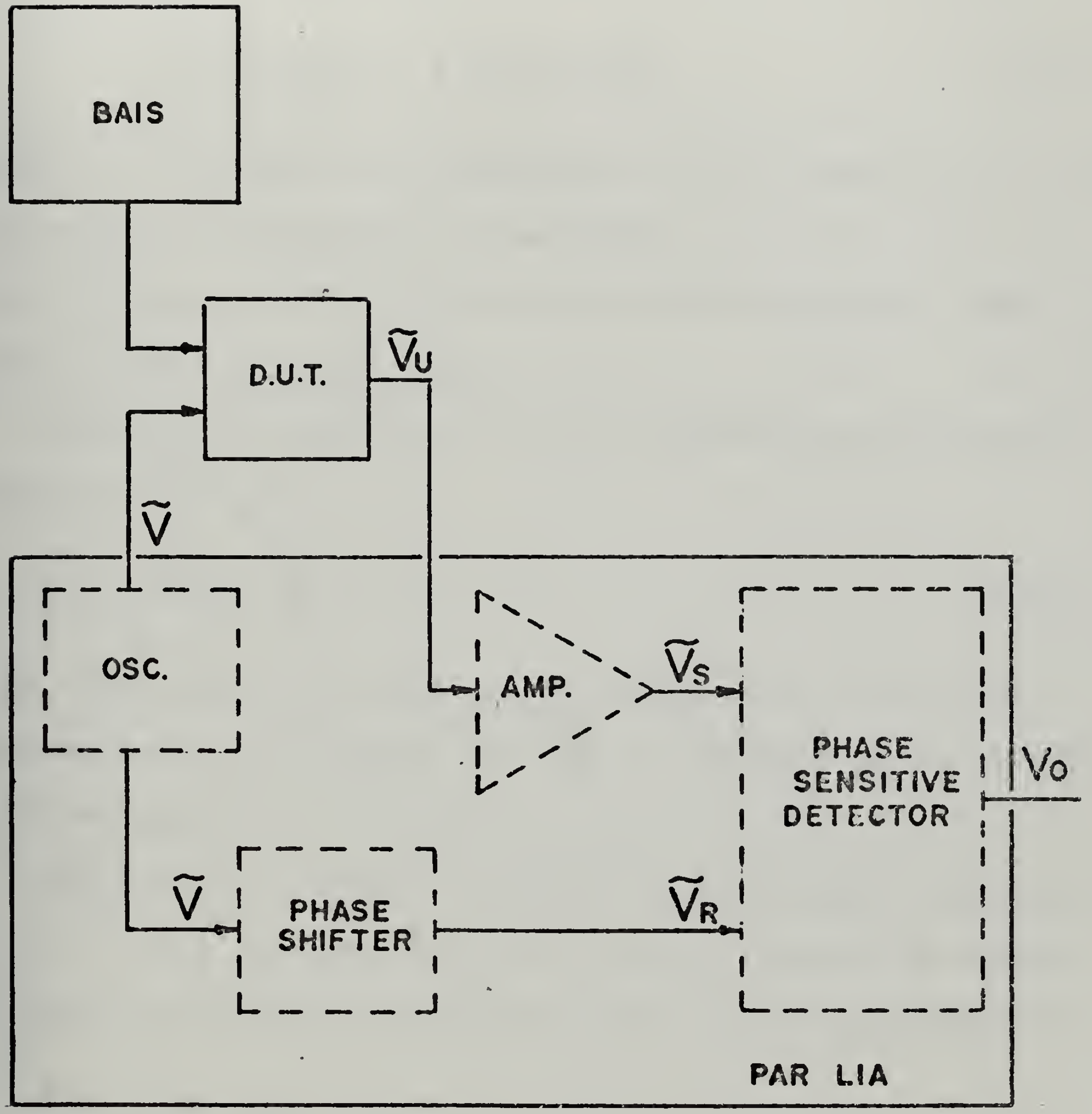
BAIS
D.U.T.
$\tilde{V}_U$
$\tilde{V}$
OSC.
AMP.
$\tilde{V}_S$
PHASE SENSITIVE DETECTOR
V_O
$\tilde{V}$
PHASE SHIFTER
$\tilde{V}_R$
PAR LIA

Figure 4-5. Equivalent Circuit for Low-Frequency Phase Sensitivity Measurements

$$V_0 = \frac{AV_{th}}{(G+G_X)^2+\omega^2(C+C_X)^2} \cdot \left\{G_X\left((G+G_X)\cos\beta-\omega C\sin\beta\right)\right.$$

$$\left. + \left(\omega(C+C_X)\cos\beta + G\sin\beta\right)\right\} \qquad (12)$$

where $Y = G + j\omega C$ is the admittance of the substrate of the MIS to ground including the amplifier; $Y_X = G_X + j\omega C_X$ is the admittance of the MIS and β is the total phase angle given by, $\beta = \phi_r - \phi_A - \phi_{th}$.

Equation 12 simplifies to the following equation when $G \gg G_X$ and $C \gg C_X$[13]

$$V_0 \doteq \left|AV_{th}\right| \frac{C_x}{C} \quad . \qquad (13)$$

Thus, the output is a measure of capacitance if the two restrictions on C_X and G_X are met. A similar result obtains for conductance.

The accuracy of Eq. 13 depends on the proper adjustment of β.[14] If β deviates from the correct value by an amount $\Delta\beta$ then the capacitance deviates from its true capacitance

$$\frac{\Delta C_X}{C_X} = \frac{G_X}{\omega C_X}\ \Delta\beta \qquad (14)$$

where the quantity $\omega C_X/G_X = Q_X$ is the quantity of the MIS. For a capacitance of 1000 pf, a resistance of 10 KΩ and a

---

[13] This relationship exists if G is on the order of 10^{-6} and C is about 1000ρ. [28].

[14] β is controlled by the LIA phase knob through ϕ_r and by the amplifier sensitivity setting through ϕ_A .

frequency of 1 KHz, Eq. 14 becomes

$$\frac{\Delta C_X}{C_X} \doteq 100\ \Delta\beta \quad . \tag{15}$$

Thus the setting of β is critical in obtaining error-free capacitance curves. On the other hand, it can be shown that $\Delta G_X/G_X \doteq .010\Delta\beta$ and apparently the conductance can be measured with little error for relatively large phase errors.

Two types of preamplifiers are useable with the LIA for C-V measurements. The Model 116 differential preamplifier requires a measuring resistor across its input to ground. The value of this measuring resistor depends on the conductance of the MIS under test. For MIS conductance of 10^{-6} ℧ the measuring resistor should have a value of approximately 100Ω. For larger conductances, the measuring resistance also increases. A measuring resistance value of 5KΩ was required on the Ge-MIS. The Model 184 photometric preamplifier is the better of the two amplifiers for three reasons. These reasons are: 1) an input signal monitor is provided, 2) it is a more sensitive current sensing amplifier which requires no measuring resistor, and 3) absolute capacitance values can be obtained by calibrating the LIA with standard capacitors. Since the 184 has a virtual ground input impedance, it can not be used with devices that show high leakage.

The LIA can also be used to give high-frequency C-V since it is sensitive to ac signal frequencies up to 210 KHz and this frequency is the high-frequency capacitance case

on many MIS (Si-MOS, for example). It can also give conductance measurements by simply changing the reference phase angle by 90°. The derivatives of the C-V and G-V curves are also obtainable with slight modification of the test circuit but were not attempted in this thesis.

V. ANALYSIS OF C-V DATA

Two computer programs were used to analyze the experimental C-V data in this research. They were originally developed for silicon MOS. It is assumed that they can be applied to germanium and the IV-VI alloy semiconductor MIS. A third program was developed to calculate the high-frequency inversion capacitance minimum for different values of semiconductor dielectric constant and different type insulators.[15]

A. COMPUTER PROGRAM TO ANALYZE THE HIGH- AND LOW-FREQUENCY C-V DATA

This program calculates and plots the following types of information from experimental high- and low-frequency C-V data: the impurity concentration at the semiconductor surface and within the bulk, plots of the variation of surface potential with respect to the gate voltage (V_S-V_a), the inputed C-V data (C-V), the inverse normalized space charge capacitance squared versus surface potential $\left((C_i/C_S)^2\text{-}U_S\right)$, the interface state density versus the semiconductor potential (N_{SS}-ψ), and the effective interface charge versus the potential drop across the semiconductor surface (Q_{eff}-V_S).

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[15] The dielectric constant of the IV-VI alloy semiconductor samples is not known exactly. Doshier, in his theoretical calculation of C-V, used 400 for this constant [8].

This program was adapted from a program developed by the University of New Mexico for analysis of Si-MOS devices for radiation vulnerability studies [28].

1. Semiconductor Surface and Applied Potential

This section and the following two sections contain only those equations necessary to allow an understanding of the computer program and, as such, the equations will not be developed in detail. Consider the differential capacitance of the MIS

$$C = \left|\frac{dQm}{dV_a}\right| \tag{16}$$

where Qm is the charge on the gate and V_a is the voltage across the device. Since the differential change in gate charge is equal to the insulator capacitance times the differential change in voltage across the insulator, the capacitance can be written as

$$C = C_i \left(1 - \frac{dV_S}{dV_a}\right) \tag{17}$$

where V_S is the voltage across the silicon surface region. By rearranging the terms and integrating, this equation becomes

$$V_S = \int_{-\infty}^{V_a} \left(1 - \frac{C}{C_i}\right) dV_a + K$$

$$= U_S + K, \text{ where } U_S \text{ is the integral.} \tag{18}$$

If the high frequency normalized capacitance is considered, so as to neglect the contribution from interface

capacitance C_{SS}, U_S becomes

$$U_S = \int_{-\infty}^{V_a} \left\{ \frac{\left(\frac{C_i^2}{C_S}\right)^{\frac{1}{2}}}{\left(\frac{C_i^2}{C_S}\right)^{\frac{1}{2}} + 1} \right\} dV_a \quad . \tag{19}$$

The quantity $(C_i/C_S)^2$ can be obtained from the experimental high-frequency data from the relation

$$\left(\frac{C_i}{C_S}\right)^2 = \left\{\left(\frac{C_i}{C_S}\right)_{HF} - 1\right\}^2 . \tag{20}$$

The $(C_i/C_S)^2 - U_S$ plot is obtained by evaluating Eqs. 19 and 20 and is the first plot drawn by the computer.

A least-squared-error fit is applied to the linear portion of this plot, if it exists.[16] From the slope of this line the surface impurity concentration can be found by

$$N_S = - 2 \frac{C_i^2}{\varepsilon \; qA^2m} \tag{21}$$

where m is the slope. In the above equations, the surface was assumed to be in depletion[17] so the surface potential

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[16] The linearity of the $(C_i/C_S)^2$ versus U_S plot is an indication of two important properties of the MIS. If the curve is not linear or is linear in two regions it may indicate an inordinate amount of interface states or a gross nonuniformity in the insulator or semiconductor.

[17] Depletion region markers showing the depletion region used are plotted on the C-V high-frequency curve output and determined by the criterion $(.05C_i + .95C_{min}) \leq C \leq (.25C_i + .75C_{min})$ where C_{min} is the minimum capacitance value.

could be considered zero and the inverse of the space charge capacitance versus V_S plot has a constant slope.

The impurity concentration in the bulk can be calculated from the following equation which is valid when the surface capacitance is at its minimum value.

$$\left|N_b\right| = n_i \exp\left(\frac{q\left|V_S\right|}{2kT}\right)\left\{2\left(\frac{q\left|V_S\right|}{kT} - 2\right)\right\}^{\frac{1}{2}} \tag{22}$$

C_{Smin} can be obtained from the experimental high frequency capacitance curve and is related to V_S by

$$\frac{kT}{n_i K_S \varepsilon_0} \cdot \left(\frac{C_{Smin}}{A}\right)^2 = \frac{\exp\left[q\left|V_S\right|/2kT\right]}{\left[2(q\left|V_S\right|/kT - 2)\right]} \tag{23}$$

With N_b calculated and using the relationship

$$\phi_b = \frac{kT}{q} \ln \frac{\left|N_b\right|}{n_i} \tag{24}$$

where ϕ_b is the potential in the bulk, the constant, K in Eq. 18, can be determined and V_S obtained as a function of V_a. This is the third plot output of the program. The program also provides tabular data of N_S, N_b and ϕ_b.

2. Interface/State Density

The interface state density can be found from the following equation

$$N_{SS} = \frac{1}{qA} C_{SS} \tag{25}$$

where N_{SS} is given in units of $[\text{volt-meters}^2]^{-1}$ and C_{SS} is found from

$$C_{SS} = \frac{C_i}{\left(\frac{C_i}{C}\right)_{LF} - 1} - \frac{C_i}{\left(\frac{C_i}{C}\right)_{HF} - 1} \qquad (26)$$

The computer solution to Eq. 25 is the fourth graph output of the program with the horizontal axis being defined as $-(\phi_b + V_S)$ and is valid only in the interval $-2\phi_b < V_S < 0$ when the semiconductor is in depletion. The program also outputs, in tabular form, three values of N_{SS} corresponding to V_S values of approximately $-2\phi_b$, $-\phi_b$ and 0.

3. Effective Interface Charge

The effective interface charge is a form of insulator charge and is given by the equation

$$Q_{eff} = \frac{C_i \quad (V_S - V_a) - Q_S}{A} \qquad (27)$$

where Q_S can be determined from experimental data as follows

$$Q_S = qK_S\varepsilon_0 A^2 \left\{ \frac{\left(\frac{C_i}{C}\right)_{HF} - 1}{C_i} \right\} \left\{ N_S - N_b \left[\exp \frac{qV_S}{kT} + 2\left(\frac{N_i}{N_b}\right)^2 \sinh \frac{qV_S}{kT} \right] \right\} \qquad (28)$$

Equation 27 is the fifth plot output from the program. Tabular data for 3 values of Q_{eff} and N_{eff} are provided for V_S values of $-2\phi_b$, $-\phi_b$ and 0.

B. COMPUTER PROGRAM BASED ON HIGH-FREQUENCY C-V DATA ONLY

There are several papers on the evaluation of MIS structures from high-frequency curves [15, 18, 30] which provides the following information: 1) conductivity type, 2) impurity concentration, 3) minority carrier lifetime and 4) interface state density. Quantities 1, 2, and 4 are obtainable directly from C-V curves. Quantity 3 is obtained from the C-t curve when a MIS is biased rapidly from accumulation to inversion. Other quantities obtainable from C-V curves at different temperatures and conditions are charge transport in the insulator, trapping effects, polarization effects, and space charge build-up due to ionizing radiation.[18] Except for the last effect these quantities will not be discussed in this thesis.

1. Conductivity Type

The determination of semiconductor conductivity type is a simple matter from a high-frequency plot. One simply observes the slope of the C-V curve as the dc bias is swept from accumulation to inversion (or vice versa). If the slope is negative, the semiconductor is p-type and if the slope is positive it is n-type. This method for determining conductivity type is faster than the Hall

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[18] The ionizing radiation effect is discussed in Chapter IX of this thesis. In that chapter C-V curves are evaluated before and after electron irradiations of a standard CN 138 N-channel depletion MOSFET.

method,[19] however, a drawback is the required insulator film deposition. A film deposition is not, of course, required in the Hall method.

2. Interface State Density

When the deviation from the ideal C-V curve is the result of surface states, a determination of these states can be found by the amount of shifting that takes place on the voltage axis of the C-V plot. A computer program that first calculates the ideal C-V curve and then compares it with input experimental C-V curves is discussed in this section [30].

The following input parameters are used: the accumulation capacitance in picofarads, the impurity concentration in cm , the temperature in degrees Kelvin, the composition X or Y (for lead-tin semiconductors), the dielectric constants for both the semiconductor and insulator, the insulator thickness in Angstroms and the experimental C-V in either normalized or absolute quantities.[20]

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[19] The Hall method has been the standard procedure for determining conductivity type. It entails applying a magnetic field across the semiconductor in which a current is flowing and measuring the Hall voltage which is set up because of carrier drift in the magnetic field. This method requires samples in the form of Hall bars and reduced temperature. A by-product, perhaps the major product, of the Hall measurement is the impurity concentration.

[20] Capacitance values in the high-frequency inversion region must be input as negative quantities.

The following quantities are the outputs of the program: the Fermi level above the valence band, the normalized high and low-frequency inversion minimum capacitance,[21] values of capacitance, values of the surface potential in volts, the energy above the valence band to which the interface states are filled in ev., and the density of interface states in cm^{-2}.

This program was used in this thesis to evaluate the cases of n-type Ge-MIS and the lead-tin alloy MIS samples whose low-frequency C-V could not be measured.

C. COMPUTER PROGRAM TO ANALYZE HIGH-FREQUENCY INVERSION MINIMUM CAPACITANCE

In the high-frequency inversion C-V case a minimum capacitance exists and is defined by the equation

$$C_{minHF} = \frac{C_i}{\frac{C_i}{C_{Sinv}} + 1} \qquad (29)$$

where $C_{Sinv} = \frac{K_S \varepsilon_0}{X_{inv}}$

and $X_{inv} = \left(\frac{4K_S \varepsilon_0 \; kT \ln (N/n_i)}{q^2 N} \right)^{\frac{1}{2}}$

---

[21] These values are presented to allow a comparison of actual versus theoretical minimum capacitance values. Their agreement depends, to a great extent, on the value of impurity concentration input.

In order to determine the combinations of K_i, K_S, N and X_i which will produce the low experimental values of C_{minHF} for the lead-tin samples, a computer program was developed to calculate C_{minHF} as a function of impurity concentration (N), insulator dielectric constant (K_i), semiconductor dielectric constant (K_S) and insulator thickness (X_i). The result of this analysis appears in Chapter VII.

VI. PREPARATION OF MIS SAMPLES OF IV-VI SEMICONDUCTORS

The device fabrication procedure is extremely critical. In the well developed silicon industry, it is relatively easy to grow or deposit an insulating layer over a silicon wafer and then vacuum deposit the metal layer. However, even with silicon, it is still difficult to produce repeatable MOS devices. When applied to IV-VI semiconducting materials, this difficulty is more severe since the MIS properties of these elements have never been studied. Methods for applying a good insulating film are not known. A good candidate is Rutile (TiO_2) whose dielectric constant is commensurate with the IV-VI semiconductors.[22] Presently Dr. N. Bottka at the Naval Weapons Center (NWC), China Lake is attempting to develop a deposition procedure for TiO_2. This section of the thesis contains the fabrication procedure for construction of the MIS samples.

A. $Pb_{1-X}Sn_XTe$ AND $Pb_{1-Y}Sn_YSe$ THIN FILM SEMICONDUCTORS

The $Pb_{1-X}Sn_XTe(Se)$ studied in this research was in the form of thin films deposited on CaF_2, BaF_2, and KCL substrates using the one-boat deposition method and the Knudson

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[22] The lead-tin semiconductors have a dielectric constant in the range of from 100 to 400. TiO_2 has a reported dielctric constant up to 100. Dielectric constants of 40 have been reported at Western Electric and a stable 80 at the University of New Mexico [12].

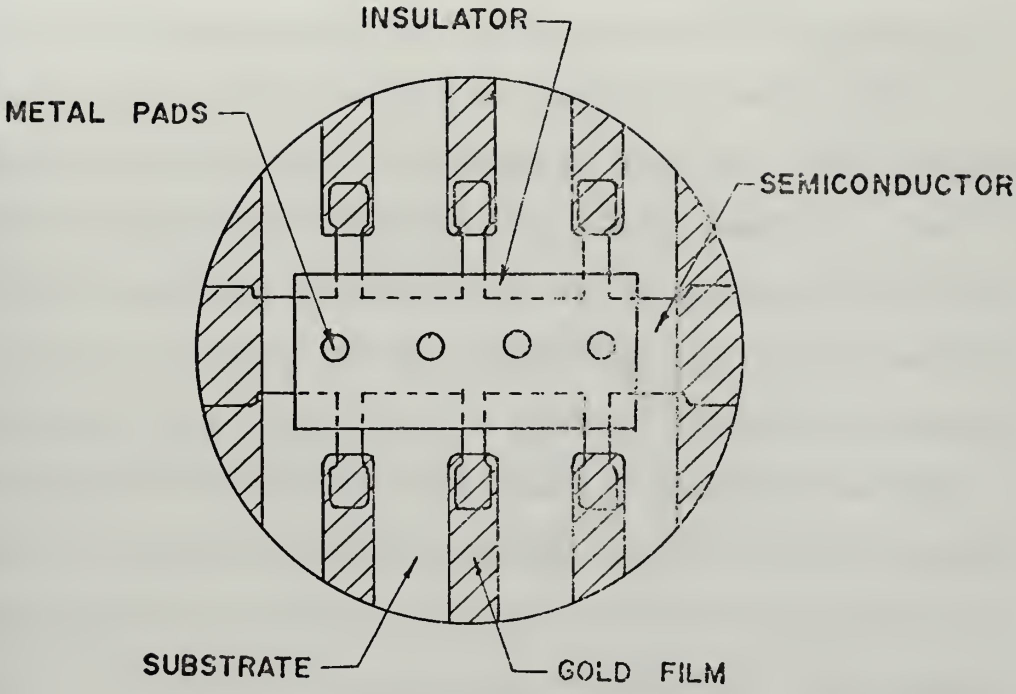
cell deposition method. Metallurgical measurements were then made on the samples in order to determine their crystal structure, orientation, and thickness. Conventional electrical measurements based on the Hall effect were then made from 300° K to 90° K to determine the carrier type, carrier concentration and Hall mobility.

The sample preparation, metallurgical evaluation and electrical measurements were not performed by the author and will not be described in this thesis. A complete description of these processes can be found in Ref. 11. Both single crystal and polycrystalline thin films were used. The mobilities of the thin films were in the range of from 80 to 29,000 $cm^2\text{-}v^{-1}\text{-}sec^{-1}$ and the concentrations (p and n) ranged from 10^{16} to 10^{18} cm^{-3}. Figure 6-1 gives the shape of the samples used: one a Hall bar for Hall measurements, the other an optical sample for optical measurements.

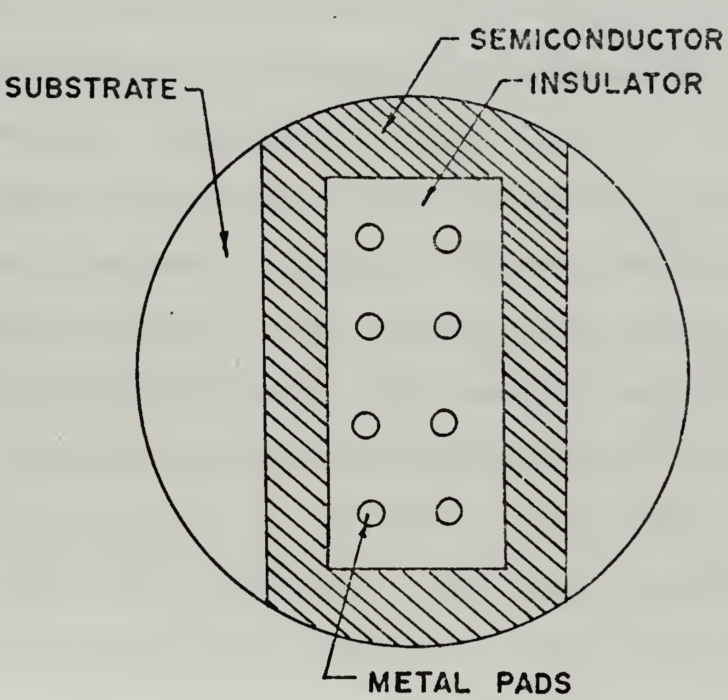
B. INSULATORS

Insulator deposition is the most critical step in producing useful MIS structures. A poor MIS causes C-V anomalities such as drift with time, non-repeatable characteristics, and low-voltage breakdown along with the possibility of having no capacitance change at all. Causes of these anomalities are pinholes through the insulator, non-uniform insulator thickness, mobile ions in insulator and interface states.

Si-MOS fabrication techniques are well established. The major insulator material used is SiO_2 and is produced by the


INSULATOR
METAL PADS
SEMICONDUCTOR
SUBSTRATE
GOLD FILM

a) Hall Sample


SEMICONDUCTOR
SUBSTRATE
INSULATOR
METAL PADS

b) Optical Sample

Figure 6-1. MIS Thin-Film Sample

oxidation of the surface of the semiconductor. For less well developed semiconductors such as the III-V and IV-VI semiconductors, other techniques had to be developed. Extensive MIS fabrication procedural work has been conducted at the University of New Mexico for GaAsP samples. Various insulator deposition methods such as RF sputtering of SiO_2, Al_2O_3, Si_3N_4 and TiO_2 and wet oxidation were tried and discarded after they were found to produce unstable insulators. The technique that proved to be most successful was the passing of atmospheric-pressure-dry oxygen over the sample at temperatures of 710° C or lower and then annealing the samples in nitrogen for more than 40 minutes. The cleanliness of the sample is critical. Mechanical lapping and polishing accompanied by chemical cleaning and polishing of the semiconductor surface before insulator deposition is an involved and complicated process [19].

The deposition scheme used for the $Pb_{1-X}Sn_XTe$ (or $Pb_{1-Y}Sn_YSe$) samples consisted of first cleaning the samples with trichloroethyne, then ethanol and finally a rinsing in heated deionized water. The samples were placed in small flasks of trichloroethyne and hand agitated for 3 minutes. The trichloroethyne was replaced in the flask by ethanol and agitated again for 3 minutes. The final cleaning step consisted of replacing the ethanol by heated deionized water and agitating before the samples were removed and dried by passing dry N_2 over them. Metal masks were then put over

the samples and loaded into the vacuum system as soon as possible to avoid surface contamination.

The deposition equipment consisted of a Norton vacuum station with a Temescal 15 KV. E-gun and Sloan deposition thickness monitor model DTM-3. The system was evacuated overnight, to approximately 10^{-7}Torr. The E-gun current was next increased slowly to out gas the evaporant and prevent sputtering.

The final step before the actual evaporation was to focus the E-beam spot size on the evaporant to ensure proper heating. With the shutter in place to prevent sporadic evaporation until the evaporant was heated properly, the E-gun was brought up to operating power which was approximately 20% of the maximum 15 KW full power. When the evaporant was observed to be properly melted and the Sloan model DTM-3 deposition thickness monitor was set to its zero level, the shutter was removed and the deposition began. The Sloan meter frequency was observed, a stop watch was started and evaporation continued for a predetermined frequency or time.[23] The sample was then allowed to cool to

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[23] The principle of operation of the DTM-3 is to mix the frequency of a stable local oscillator in the meter with the frequency of a crystal oscillator in the deposition jar, whose frequency is dependent on the amount of mass on it. The beat frequency of these two oscillators determines the thickness of the film deposited by the following formula:

$$T = \frac{2\Delta f}{p}$$

where:
T = thickness in Angstrons
Δf = beat frequency
p = density of deposited material

room temperature which took typically 1 hour and the films were checked for physical characteristics. Table I provides a list of the samples prepared and the materials used for insulator. Adhesion properties on all samples were good except for ZnS. The insulator surface appeared to contain a fair but not inordinate amount of obvious pinholes.

Semiconductor	Insulator	Thickness (A°)
$Pb_{1-X}Sn_XTe$ (Se)	Al_2O_3	100
"	Al_2O_3	300
"	Al_2O_3	980
"	SiO_2	450
"	ZnS	1000[24]
"	TiO_2	500[25]
Ge (p)	Al_2O_3	250
Ge (n)	Al_2O_3	180
Si	SiO_2	1000[26]

Table I. List of MIS Samples Prepared for Experimentation

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[24] ZnS was deposited by thermal heating in the Physics Laboratory at the Naval Postgraduate School with the help of Mr. Donald Spiel.

[25] TiO_2 has not yet been deposited; however, the deposition technique is being developed by Dr. Botka at NWC, China Lake.

[26] The SiO_2 over silicon was grown at Stanford University.

C. METAL DEPOSITION

Metal deposition was in the form of Ni pads thermally deposited through various shaped masks. The various shaped masks afforded the opportunity to observe the effect of different gate areas on experimental curves. Deposition was performed similar to the above procedure. Depending on the thickness of evaporant required, in this case two small one-quarter inch pieces of 50 mil wire, the evaporant was put in a boat and thermally heated first to form the two pieces into a single bead and to out gas and then finally to evaporate when the proper vacuum of 10^{-6} was reached. Thickness was monitored by measuring the evaporant resistance across a 2 by 5 cm area. When this resistance reached 1 KΩ, the evaporation process was terminated. In all cases the evaporated metal adhered properly. In several cases the metal was barely visible because of its thinness.

Three other type metal gates were used. On the Si sample 30 mil. and 20 mil diameter aluminum gates were deposited. On other samples no metal deposition was made and a small drop of Hg[27] was put on the tip of a probe to act as a metal gate. The Hg probe was also used on several samples which had other Ni metalization which because of the thinness of the sample, allowed the point probe to punch through the metal. The third type of metallization was in

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[27] Here there was a problem defining the area accurately since the area depended on the force applied to the mechanical probe.

the form of Au gates of 30 mil. diameter and on several Hall samples in the form of strips covering the Hall bars. The gold deposition did not adhere well. The Hg probe has given more repeatable results.

VII. EXPERIMENTAL RESULTS OF IV-VI ALLOY SEMICONDUCTOR MIS

The experimental results of IV-VI alloy semiconductor MIS are presented in this chapter. These results consist primarily of high-frequency C-V curves. The low-frequency and C-t response were considered, attempted but not presented, except in one case for each, since successful plots were not obtained. Several G-V plots were also attempted.

A. MIS SAMPLES STUDIED

MIS samples of 6 different IV-VI semiconductors were experimentally investigated. Two different types of insulators of three thicknesses were used. These combinations were: PbTe with Al_2O_3 and SiO_2, $Pb_{.82}Sn_{.18}Te$ with Al_2O_3, $Pb_{.80}Sn_{.20}Te$ with Al_2O_3 and SiO_2, $Pb_{.76}Sn_{.24}Te$ with Al_2O_3, PbSe and $Pb_{.97}Sn_{.03}Se$ with Al_2O_3, and $Pb_{.90}Sn_{.10}Se$ with SiO_2. They are also listed in Tables II and III. The major portion of the measurements were made at room temperature. Several samples were tested at liquid nitrogen temperature.

Since most of the samples showed leakage through the insulator, the measurement method using the lock-in-amplifier was not useable and, consequently, only a few low-frequency C-V measurements have been obtained. G-V plots were also attempted on several samples but only one successful curve was obtained.

B. HIGH-FREQUENCY C-V RESULTS

This section contains the experimental high-frequency C-V measurements at room temperature and at liquid nitrogen temperature and some low-frequency data. A theoretical C-V curve is first presented and followed by the experimental curves.

1. $Pb_{1-X}Sn_XTe$ MIS C-V curves at Room Temperature

The theoretical C-V curves for the PbTe and Pb $Pb_{0.8}Sn_{0.2}Te$ MIS samples at 300°K is presented in Figs. 7-1 and 7-2. The material parameters selected are the following: impurity concentration assumed was $1X10^{18}$ cm^{-3}, semiconductor dielectric constant assumed was 400. The high frequency C-V experimental data are presented as follows.

MIS Semiconductor	MIS Insulator and Thickness (A°)	Figure Number
PbTe	Al_2O_3 (100)	7-3
	SiO_2 (450)	7-4
$Pb_{.82}Sn_{.18}Te$	Al_2O_3 (300)	7-5
$Pb_{.80}Sn_{.20}Te$	Al_2O_3 (100)	7-6
	Al_2O_3 (300)	7-7
	SiO_2 (450)	7-8
$Pb_{.76}Sn_{.24}Te$	Al_2O_3 (100)	7-9
	Al_2O_3 (300)	7-10

Table II. $Pb_{1-X}Sn_XTe$ Semiconductor MIS Experimentally Investigated

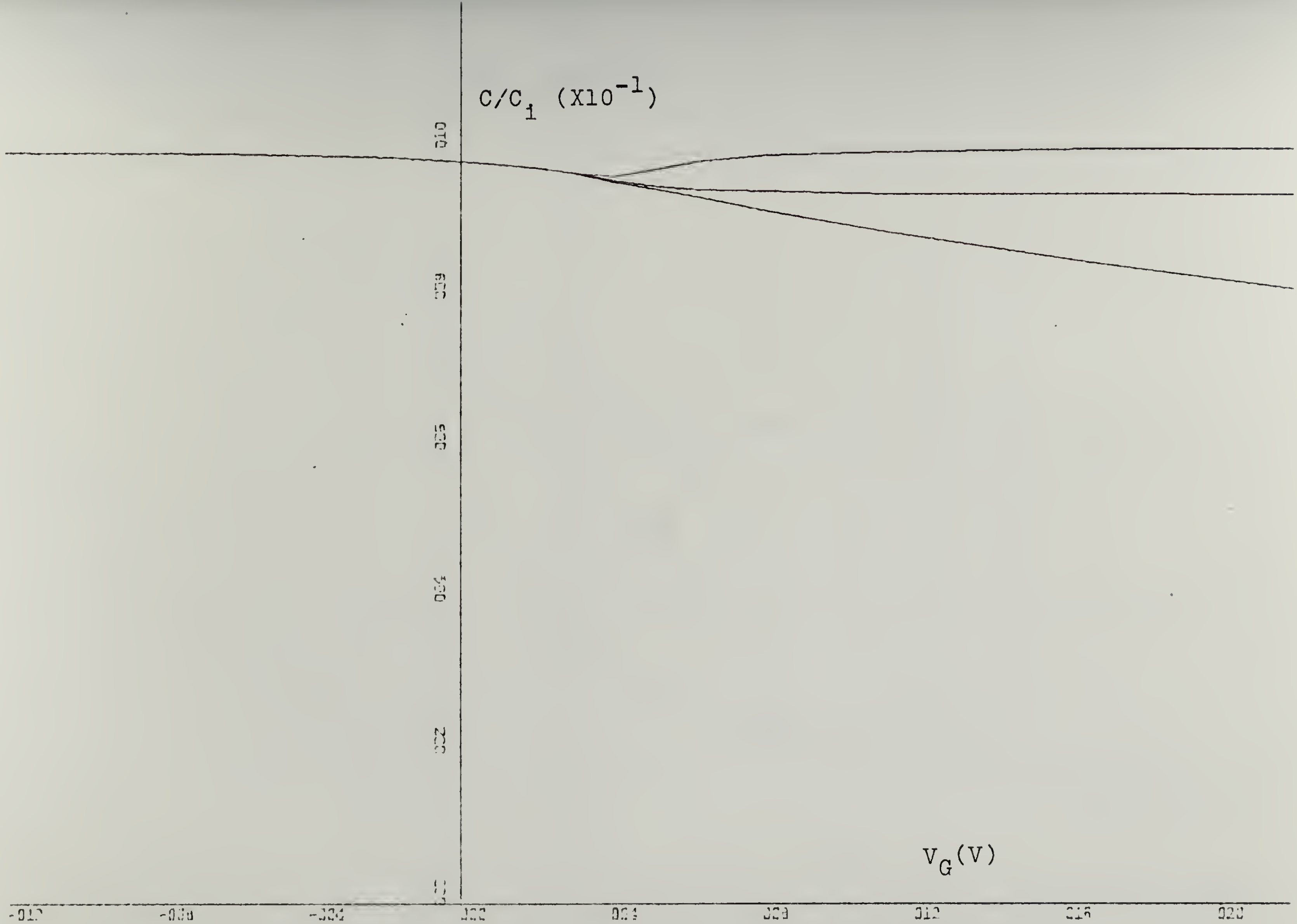

Figure 7-1. Theoretical C-V Curve for PbTe MIS (Ideal), $N = 1X10^{18}\ cm^{-3}$, $T = 300°K$, Insulator: Al_2O_3 (100A°)

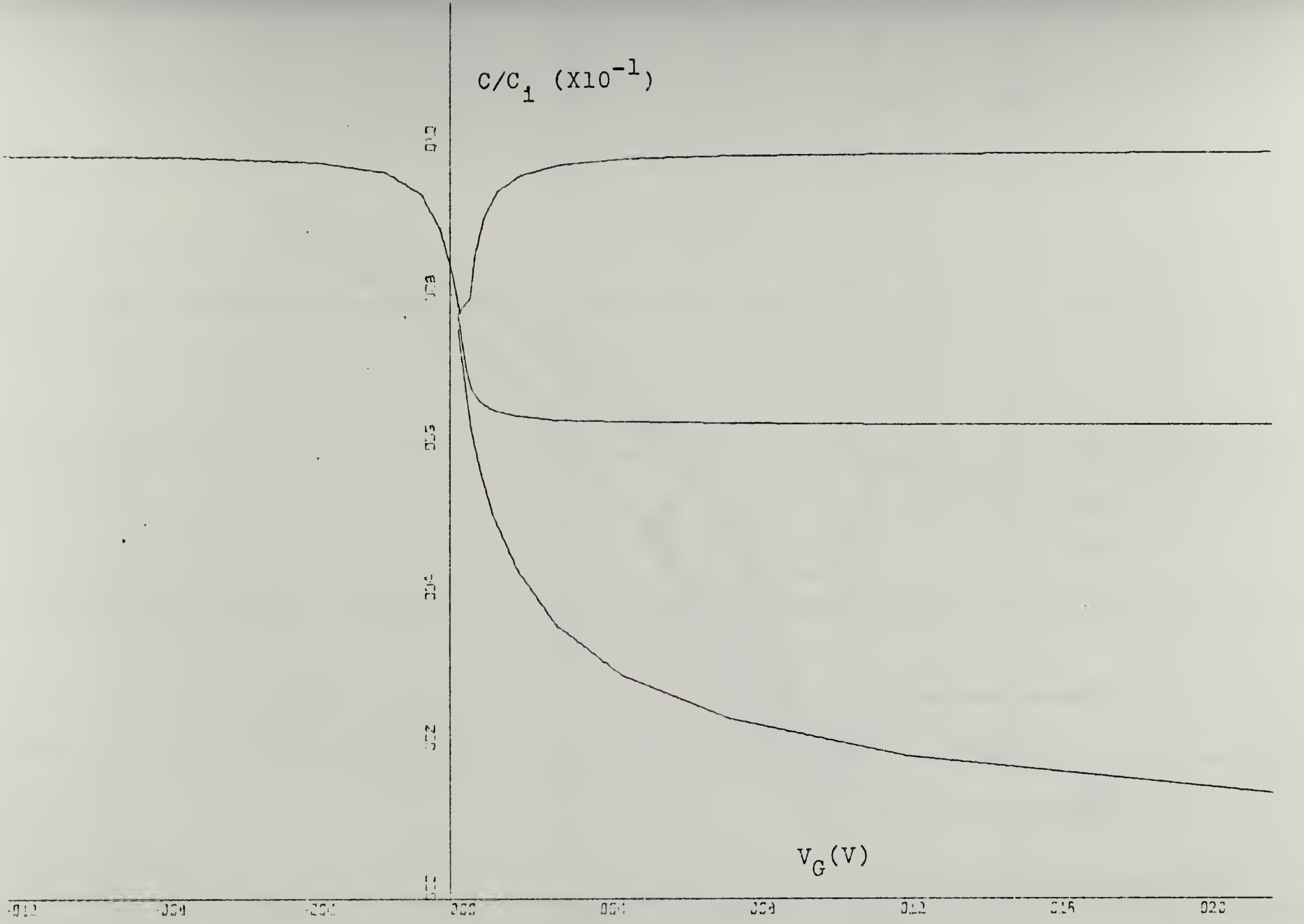

Figure 7-2. Theoretical C-V Curve for Pb$_{.80}$Sn$_{.20}$Te MIS (Ideal), N = 1X10^{18} cm^{-3}, T = 300°K, Insulator: SiO$_2$(450A°)

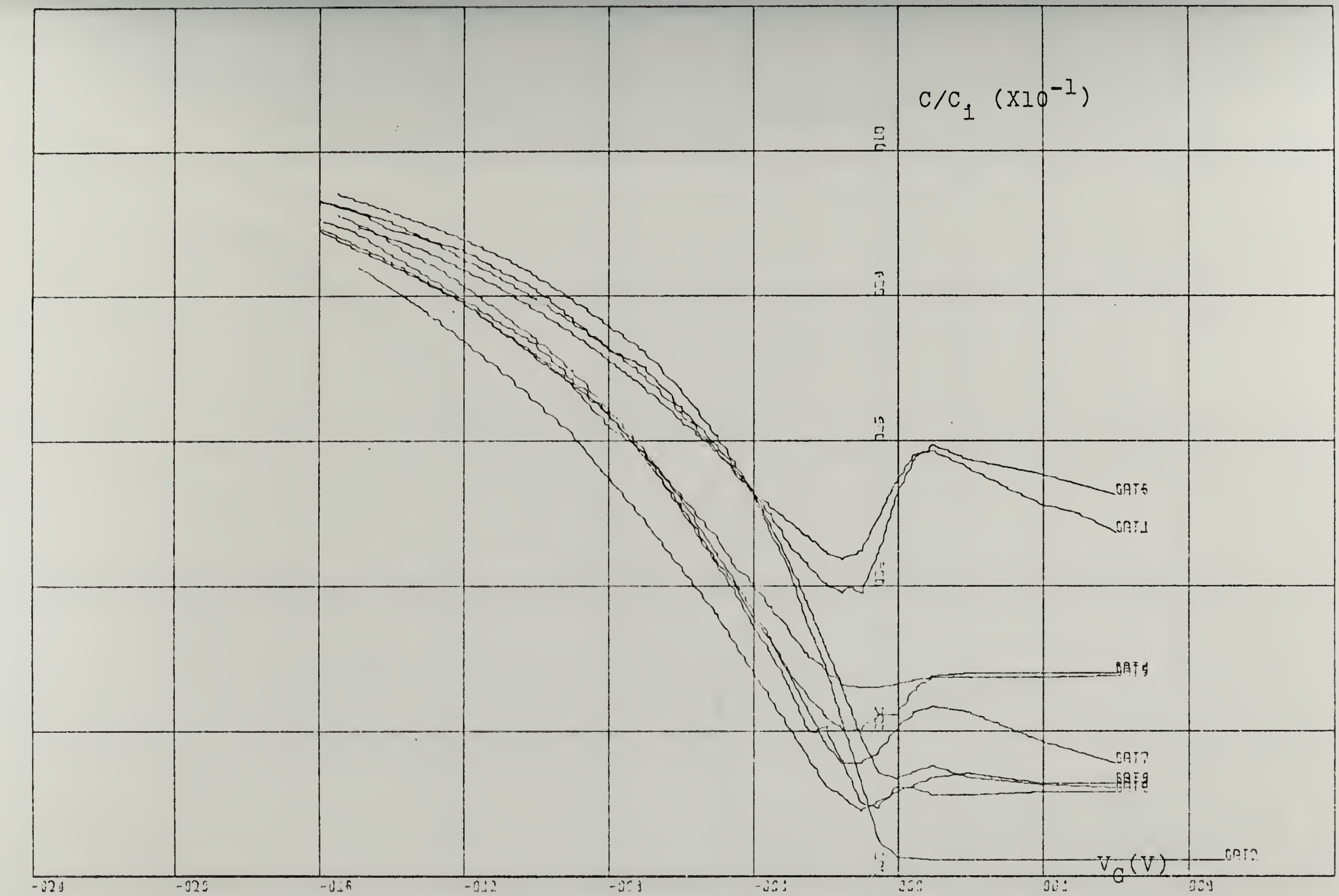

Figure 7-3. Experimental C-V Curve for PbTe MIS, T = 300°K, Insulator: Al_2O_3 (100A°)

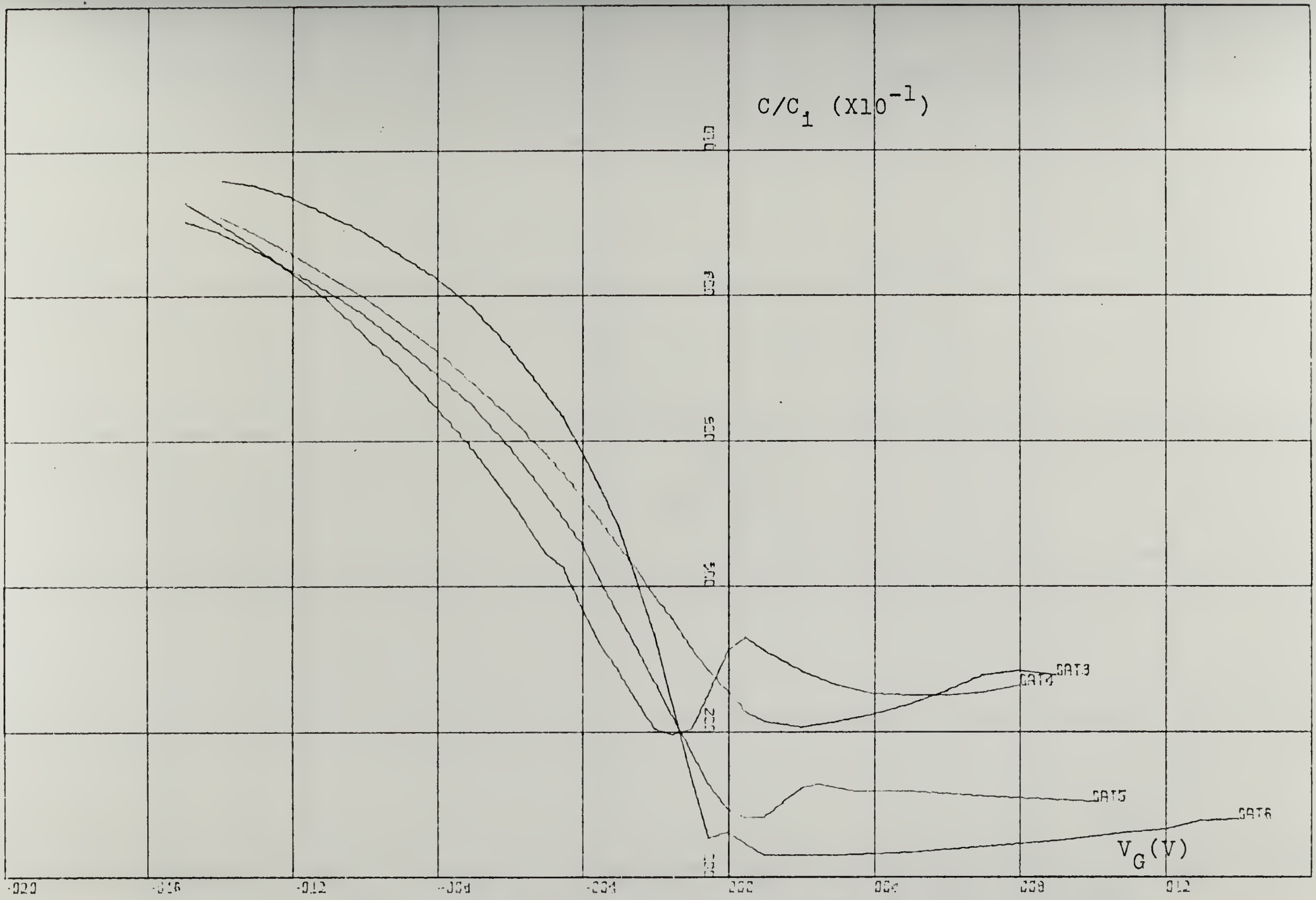

Figure 7-4. Experimental C-V Curve for PbTe MIS, T = 300°K, Insulator: SiO_2 (450A°)

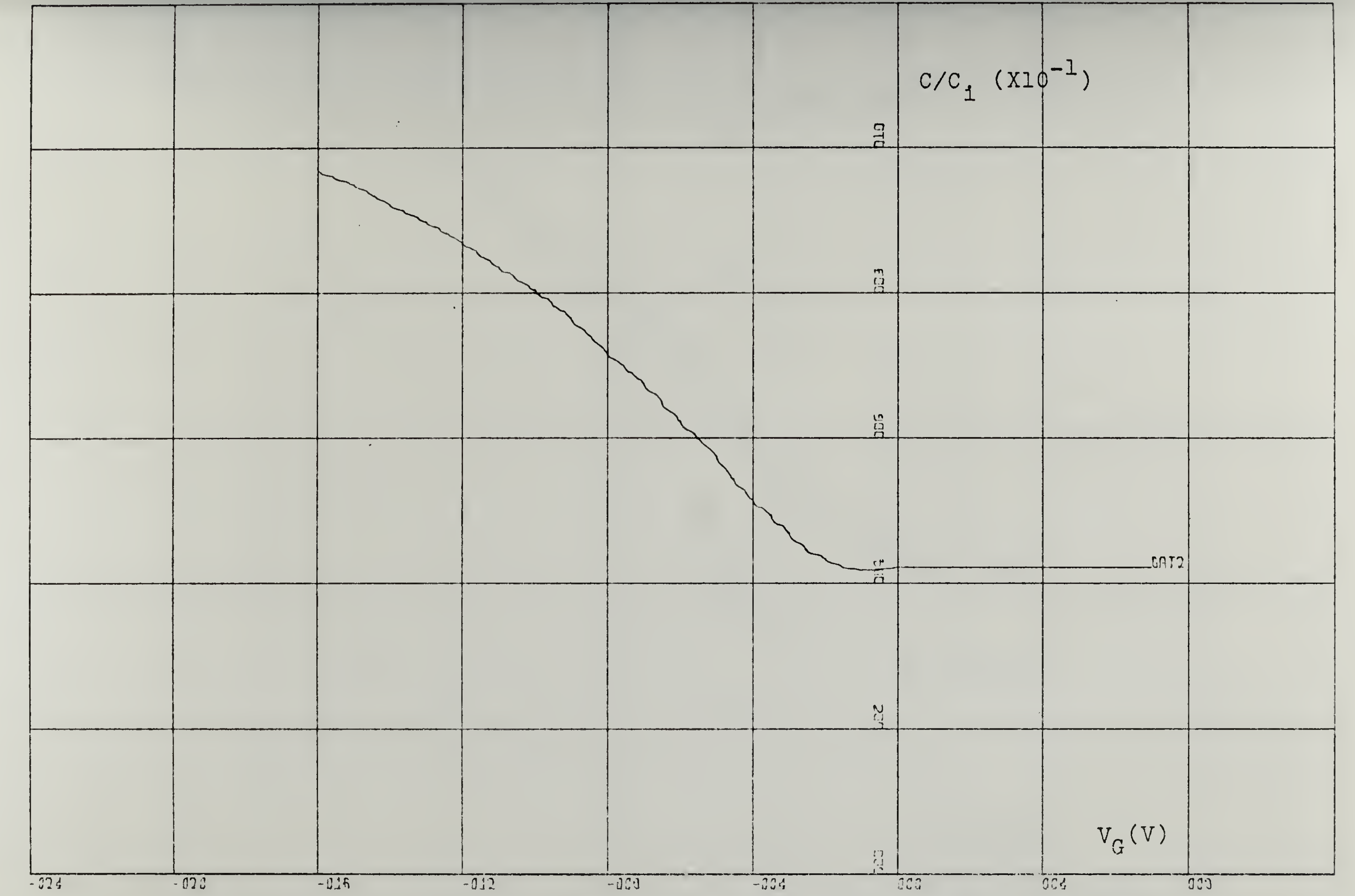

Figure 7-5. Experimental C–V Curve for $Pb_{.82}Sn_{.18}Te$ MIS, T = 300°K
Insulator: Al_2O_3 (300A°)

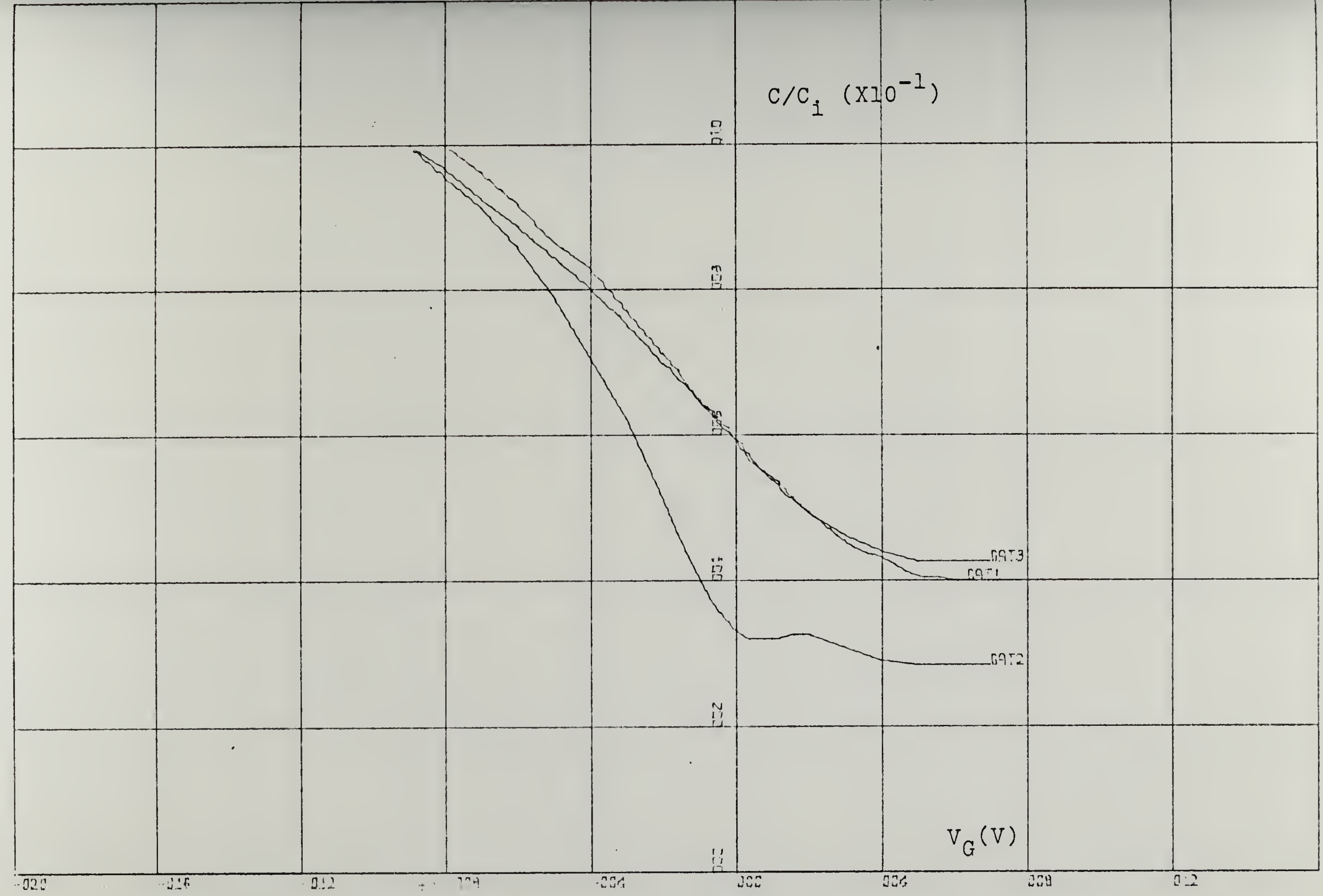

Figure 7-6. Experimental C-V Curve for $Pb_{.80}Sn_{.20}Te$ MIS, T = 300°K
Insulator: Al_2O_3 (100A°)

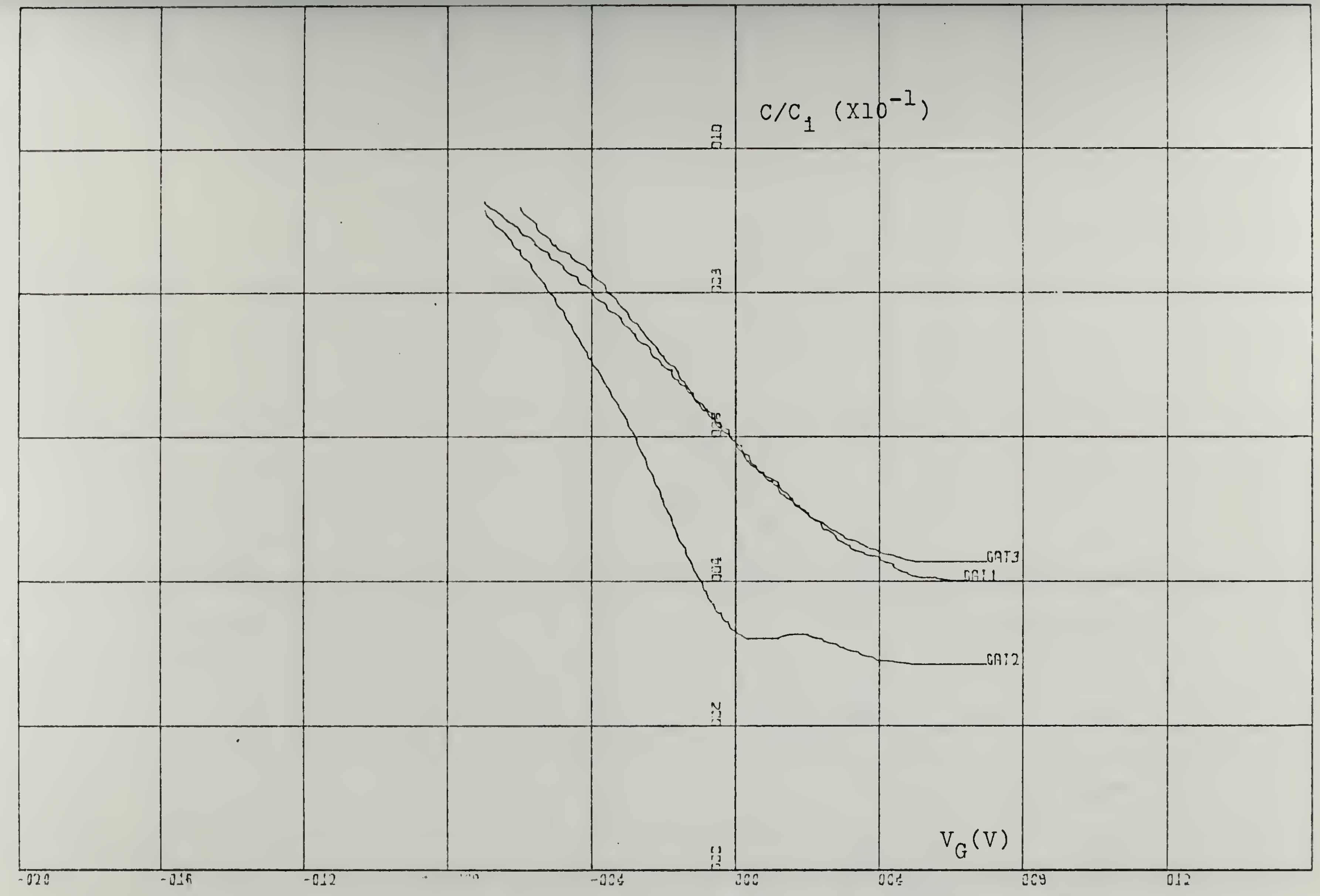

Figure 7-7. Experimental C-V Curve for $Pb_{.80}Sn_{.20}Te$ MIS, T = 300°K, Insulator: Al_2O_3 (300A°)

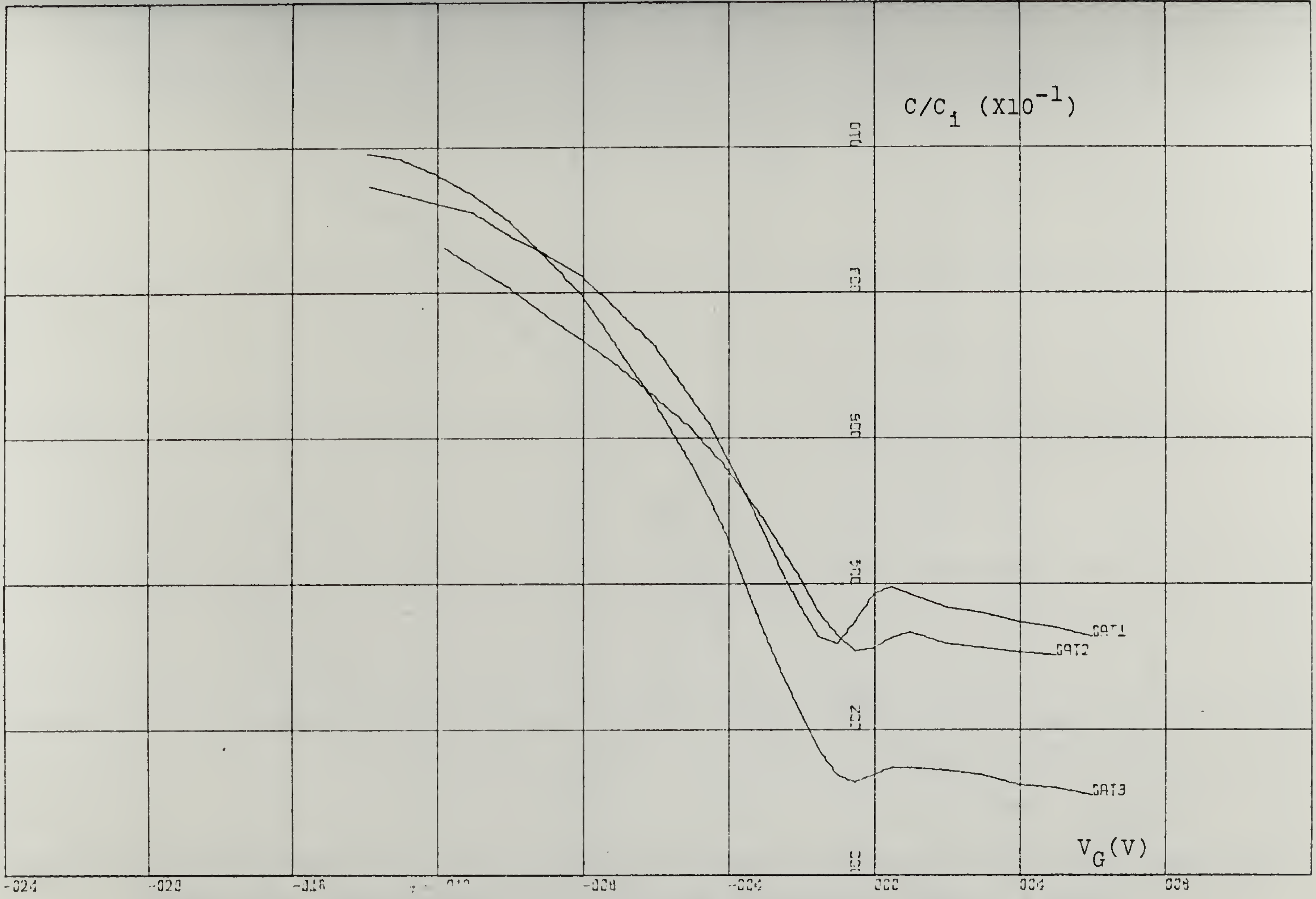

Figure 7-8. Experimental C-V Curve for $Pb_{.80}Sn_{.20}Te$ MIS, T = 300°K, Insulator: SiO_2 (450A°)

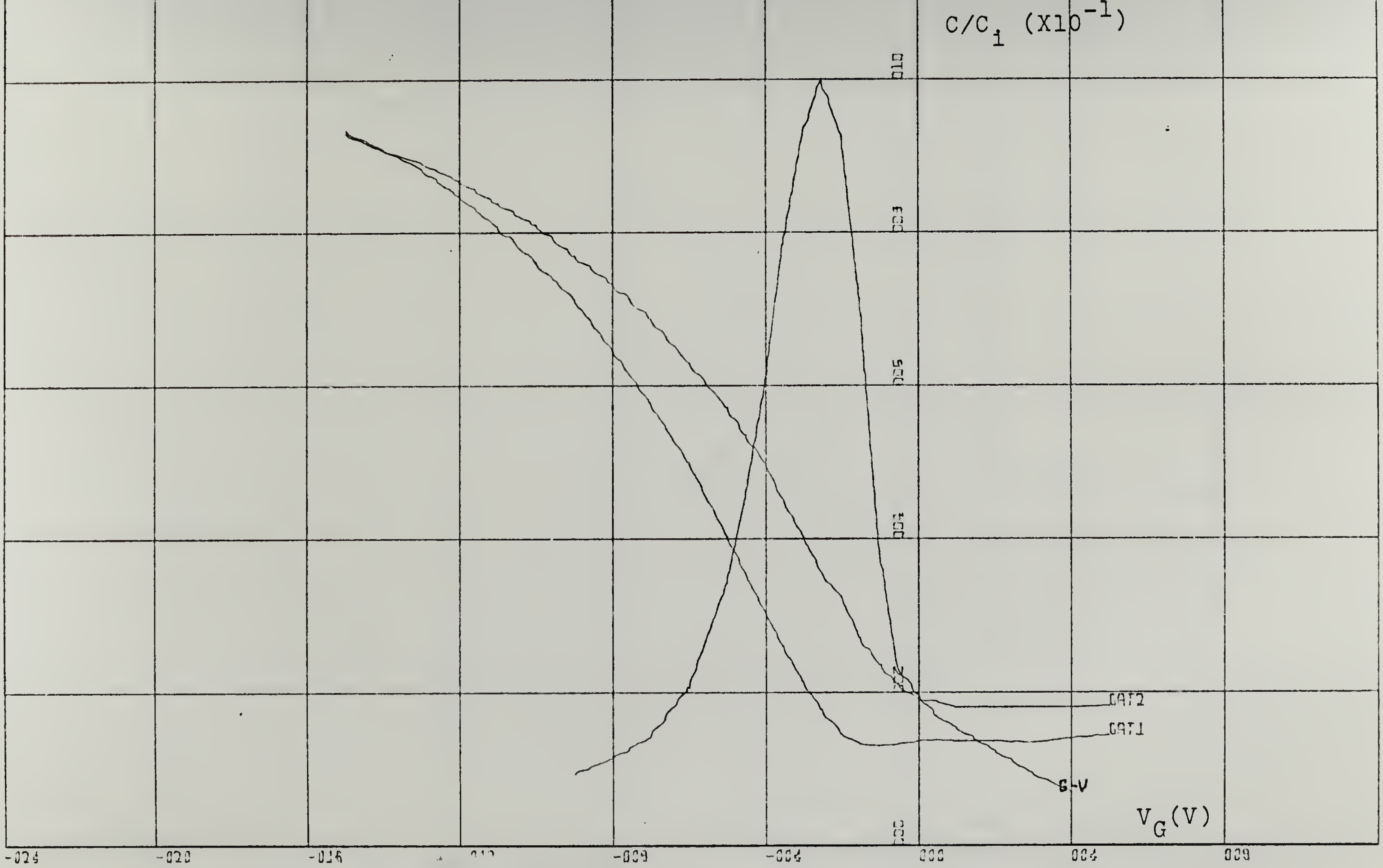

Figure 7-9. Experimental C-V Curve for Pb$_{.76}$Sn$_{.24}$Te MIS, T = 300°K, Insulator: Al_2O_3 (100A°)

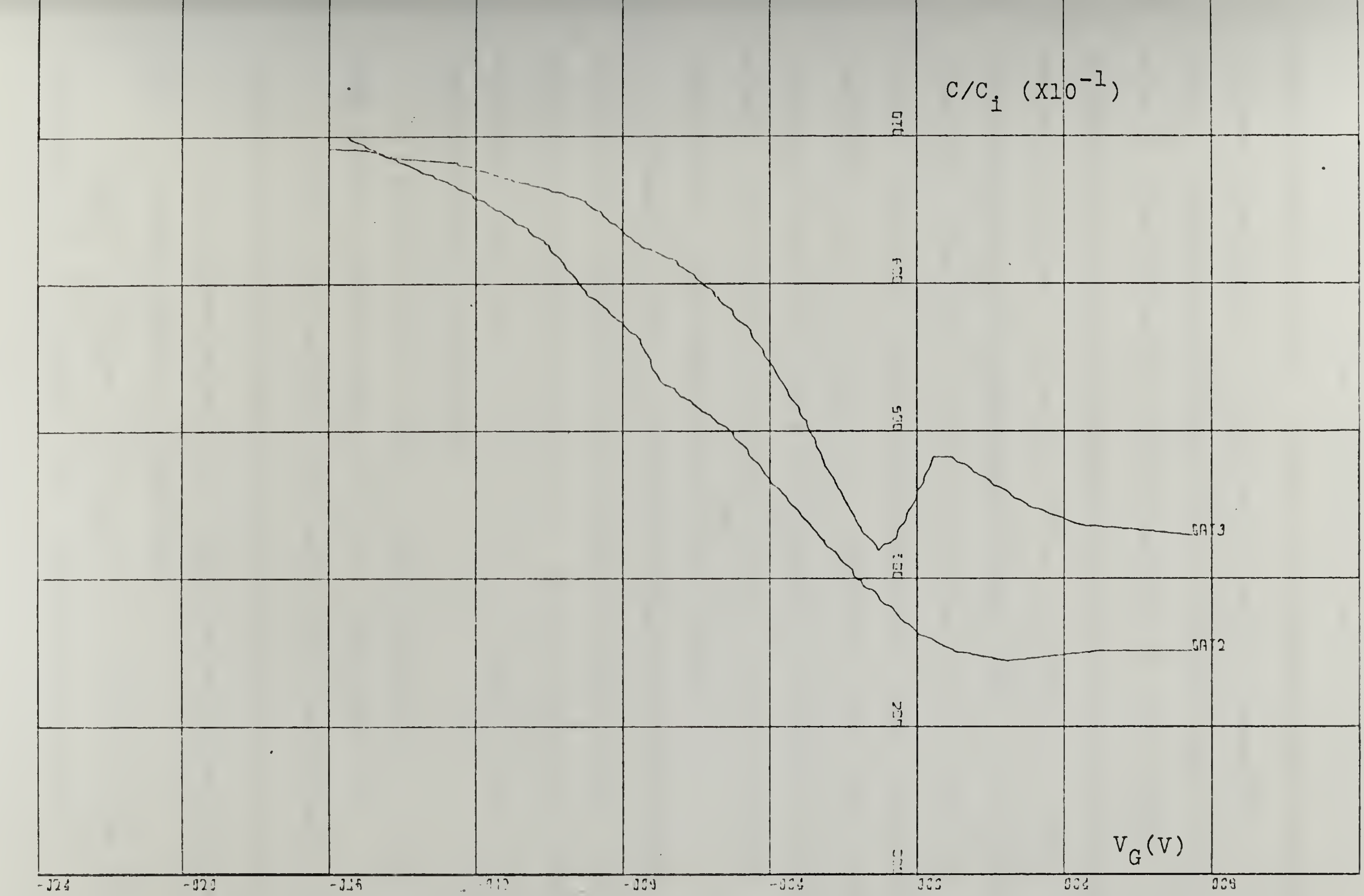

Figure 7-10. Experimental C-V Curve for $Pb_{.76}Sn_{.24}Te$ MIS, T = 300°K, Insulator: Al_2O_3 (300A°)

There are several differences between theoretical and experimental curves. First, the measured high-frequency minimum capacitance is much lower than the theoretical value. Possible explanations for this capacitance difference are the following: nonuniformities in the insulator or semiconductor, the semiconductor dielectric constant may not be as high as 400, error of the impedance measurement in the determination of capacitance brought out by the leaky insulator. The latest factor was discussed in detail in Chapter V and is, in most probability, the major cause for the differences. Although this difficulty with leaky insulators exists and the curves are distorted, depletion and inversion layers which were controlled by the gate voltage seem evident from these experimental results.

Second, drift was common in almost all the samples. Drift is not included in these figures except in Fig. 7-6 where it is presented for gate 3. Third, hysteresis effects sometimes were found. Their effects were generally not large and are not presented.

Fourth, there is often a small hump in the C-V curve near zero as shown in Figs. 7-3, 7-4, 7-8, and 7-10.

Fifth, the voltage bias ranges from the accumulation to inversion is much larger than the theoretical results.

Sixth, low-frequency and high-frequency deep depletion C-V curves can not be obtained.

Figure 7-9 shows a G-V curve in addition to the high-frequency C-V of a sample. G-V measuremnnts were not

attempted in general, since G-V curves do not provide as much information about the sample MIS as C-V curves do. Future success with G-C curves could prove to be of value if low-frequency curves are not possible. Errors associated with phase-setting on the LIA G-V curves for leaky insulator MIS is not as critical as it is in C-V curves. This was discussed in Chapter V.

2. $Pb_{1-X}Sn_XTe$ MIS C-V Curves at Liquid Nitrogen Temperature

Considerable difficulty was experienced in obtaining low-temperature C-V curves. First, Hg freezes at liquid nitrogen temperature and the measurements become irratic in many cases. Second, the samples were immersed in the liquid nitrogen in the cold thermos and the bubbling of the liquid nitrogen near the sample caused jitter in the measurement.

Figure 7-11 shows the temperature variation of the high-frequency C-V of a PbTe(Al_2O_3)MIS. The lowest temperature is labeled T1 in the figure. The accumulation capacitance was found to decrease with temperature. It contradicts the theory which asserts that accumulation capacitance remains constant for all temperatures. Instead, the inversion capacitance should decrease with temperatures since the minority carrier lifetime is reduced. This abnormality of temperature variation was not characteristic of all the samples. Another sample, Fig. 7-12, for example, shows two

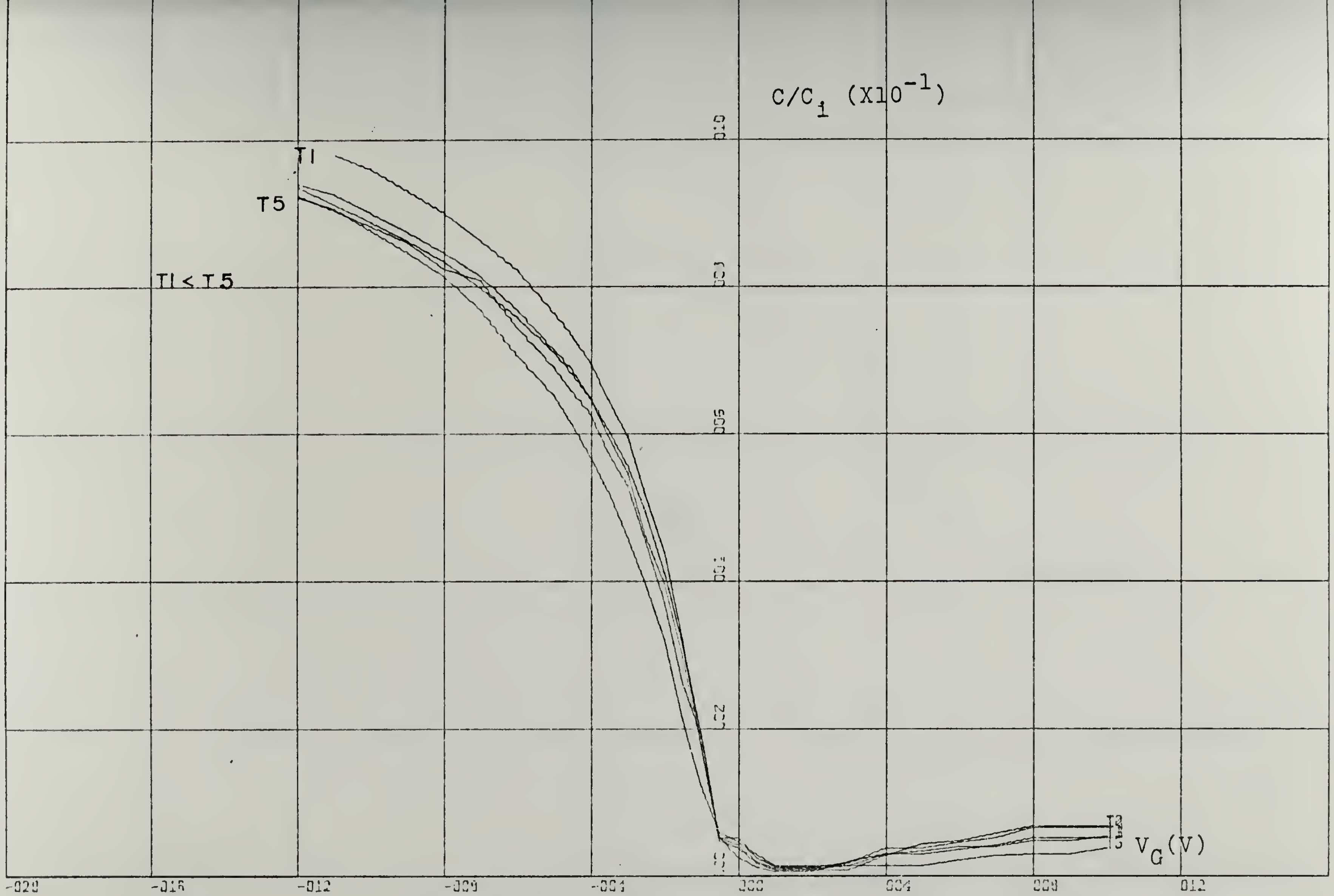

Figure 7-11. Experimental C-V Curve for PbTe MIS at Various Low Temperatures, Insulator: Al_2O_3 (300A°)

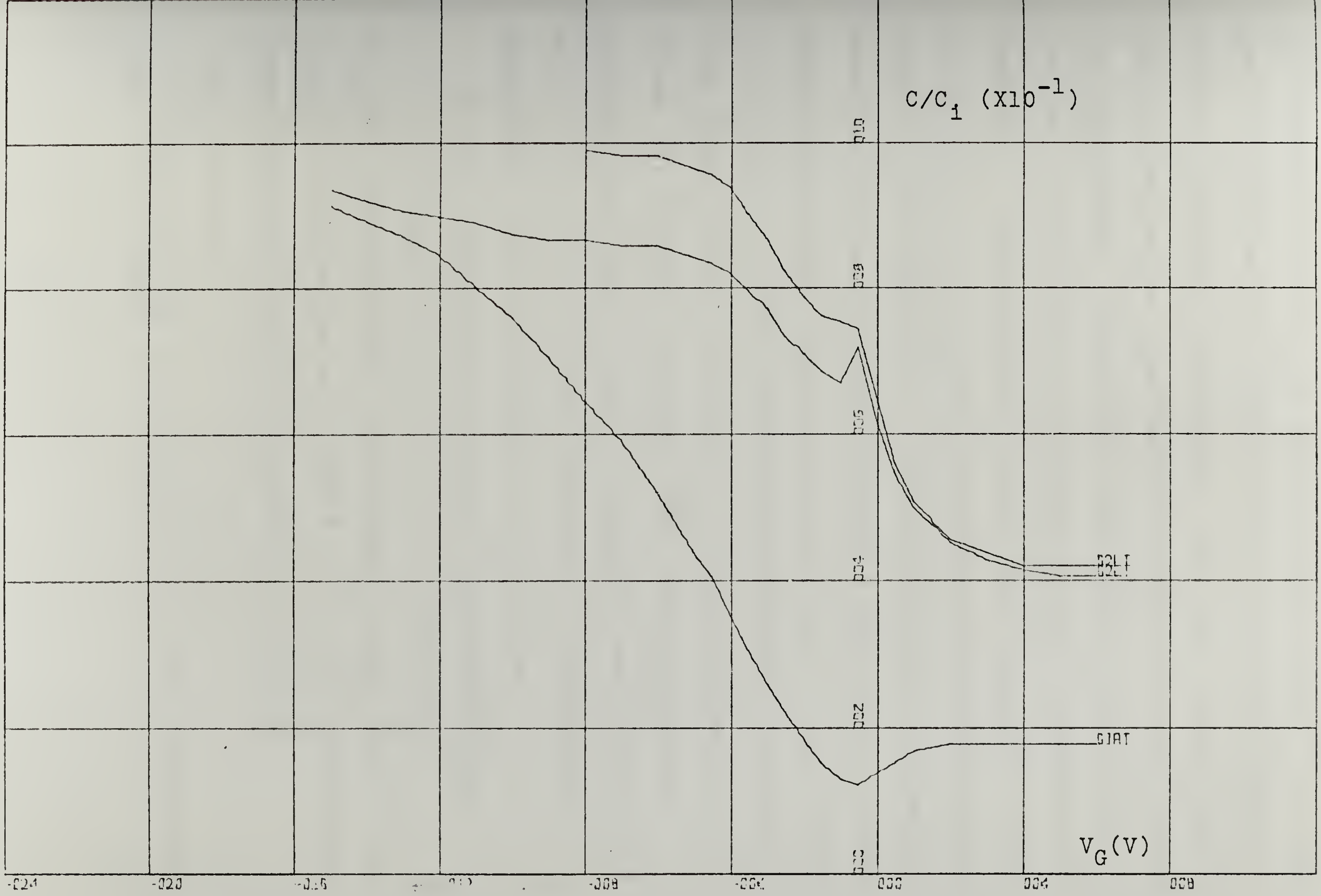

Figure 7-12. Experimental C-V Curve for PbTe MIS, T = 80°K, T = 300°K for Gate 1, Insulator: Al_2O_3 (100A°)

low-temperature curves for different gate areas.[28] In this case the trend was the opposite and the inversion capacitance went down with temperature. This fact is not clear in Fig. 7-12 since the capacitance is normalized to the insulator capacitance. The absolute capacitance values in this case were 6 picofarads in accumulation and 2 picofarads in inversion. The accumulation capacitance represents a drastic reduction of the typical measured accumulation capacitance at room temperature. The major difference present in these curves over the room temperature case was the percentage change between accumulation and inversion capacitance. In the majority of the room temperature cases, the percentage change was 40%. The reason for this difference is unknown. In general, low-temperature curves have been difficult to obtain. Since the lead-tin semiconductor MIS will be operated at cooled temperature, low-temperature measurement must be determined in the future.

3. $Pb_{1-Y}Sn_YSe$ MIS C-V Curves at Room Temperature

The theoretical C-V curves at 300°K for a $Pb_{0.9}Sn_{0.1}Se$ (SiO_2-450A°) is presented in Fig. 7-13. The carrier concentration was $1.0X10^{18}$ cm^{-3}. The high-frequency experimental C-V curves are presented as follows:

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[28] Gate 1 in Fig. 7-12 represents the room temperature case for the sample.

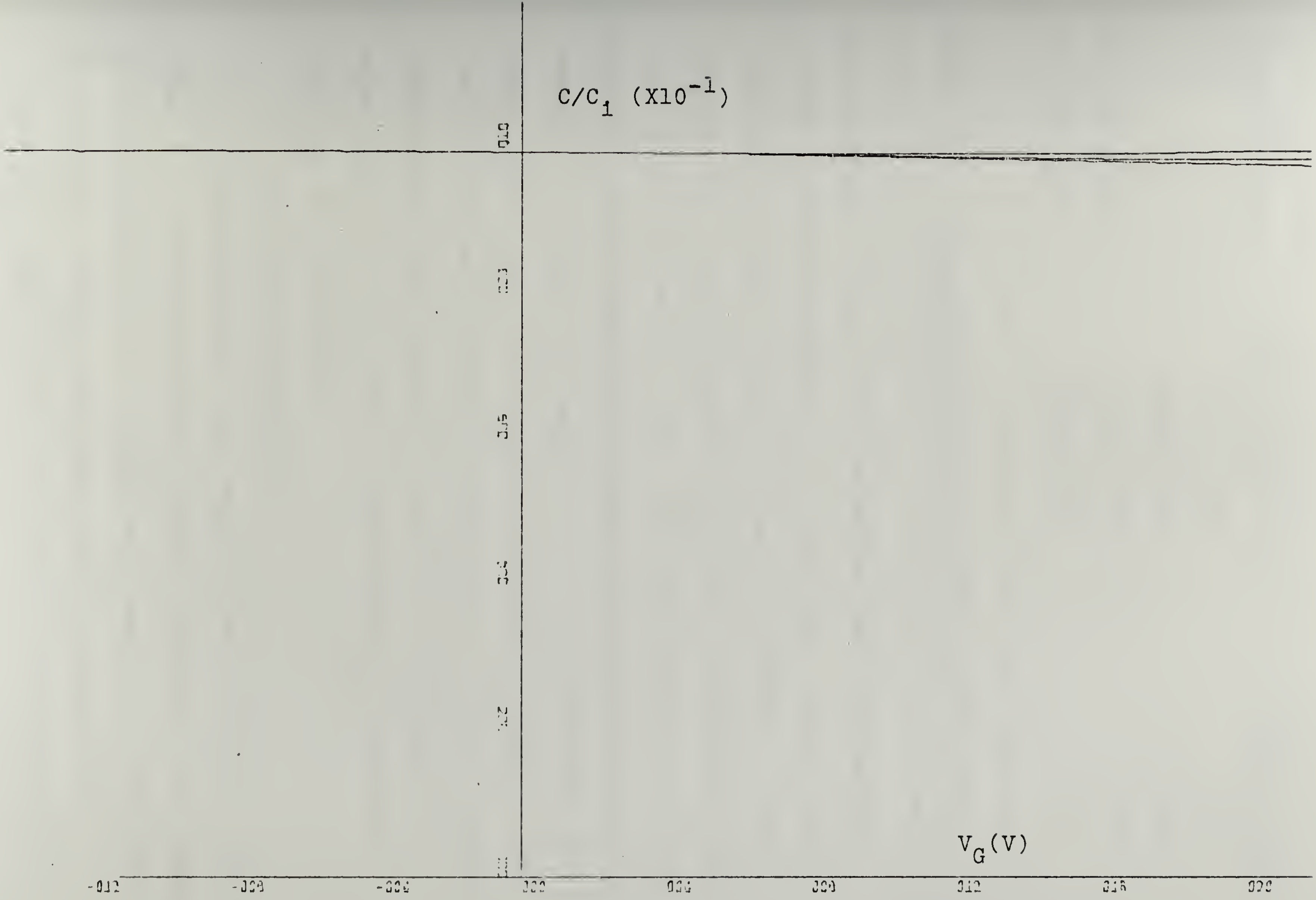

Figure 7-13. Theoretical C-V Curve for $Pb_{0.9}Sn_{0.1}Se$ MIS (Ideal), $N = 1X10^{18}$ cm^{-3}, T = 300°K, Insulator: SiO_2 (450A°)

MIS Semiconductor	MIS Insulator and Thickness (A°)	Figure Number
PbSe	Al_2O_3 (300)	7-14
	Al_2O_3 (300)	7-15
$Pb_{.97}Sn_{.03}Se$	Al_2O_3 (300)	7-16
$Pb_{.90}Sn_{.10}Se$	SiO_2 (450)	7-17

Table III. $Pb_{1-Y}Sn_YSe$ Semiconductor MIS Experimentally Investigated

The difference between the theoretical and experimental curves is obvious from Figs. 7-13 and 7-14. These differences are the same as those discussed for PbSnTe; however, they are even larger because of the small capacitance variation in the theoretical curve. All experimental C-V curves contain a large capacitance change from accumulation to inversion. The only low-frequency C-V curve obtainable appears in Fig. 7-15 for a PbSe (Al_2O_3-300A°) sample. The low-frequency was obtained at 10KHz, but it is not the true low-frequency curve since the inversion and accumulation capacitances are not equal. Lower frequency curves were tried but not obtainable.

4. $Pb_{1-Y}Sn_YSe$ C-t Response

The capacitance time response was attempted. But, because of the short minority carrier lifetime of the samples at room temperature, no results were measurable except for a few cases. Figure 7-18 gives the C-t response for $Pb_{.90}Sn_{.10}Se$ pulsed from -15.V to 0.V at room temperature.

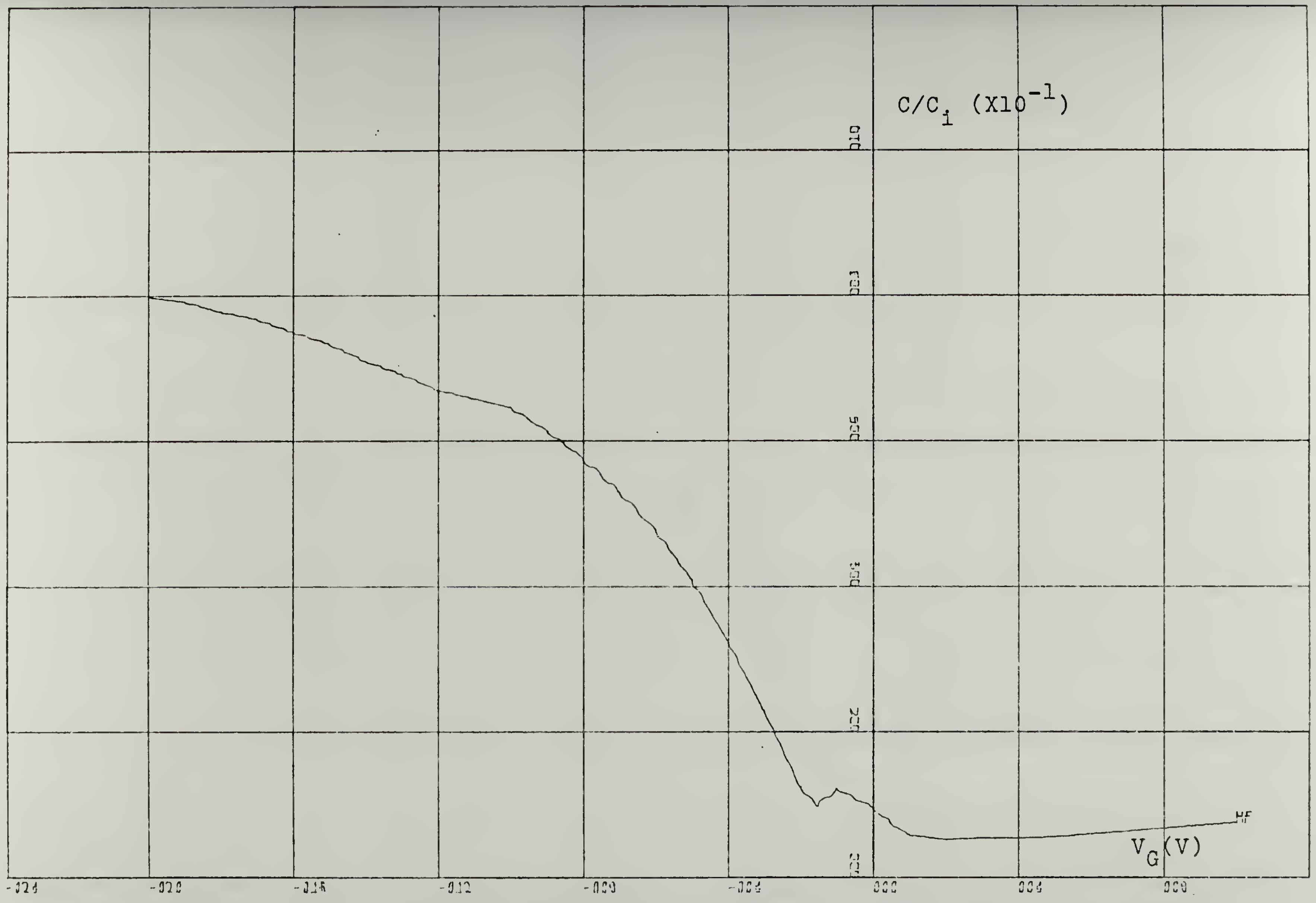

Figure 7-14. Experimental C-V Curves for PbSe #1, T = 300°K, Insulator Al_2O_3 (300A°)

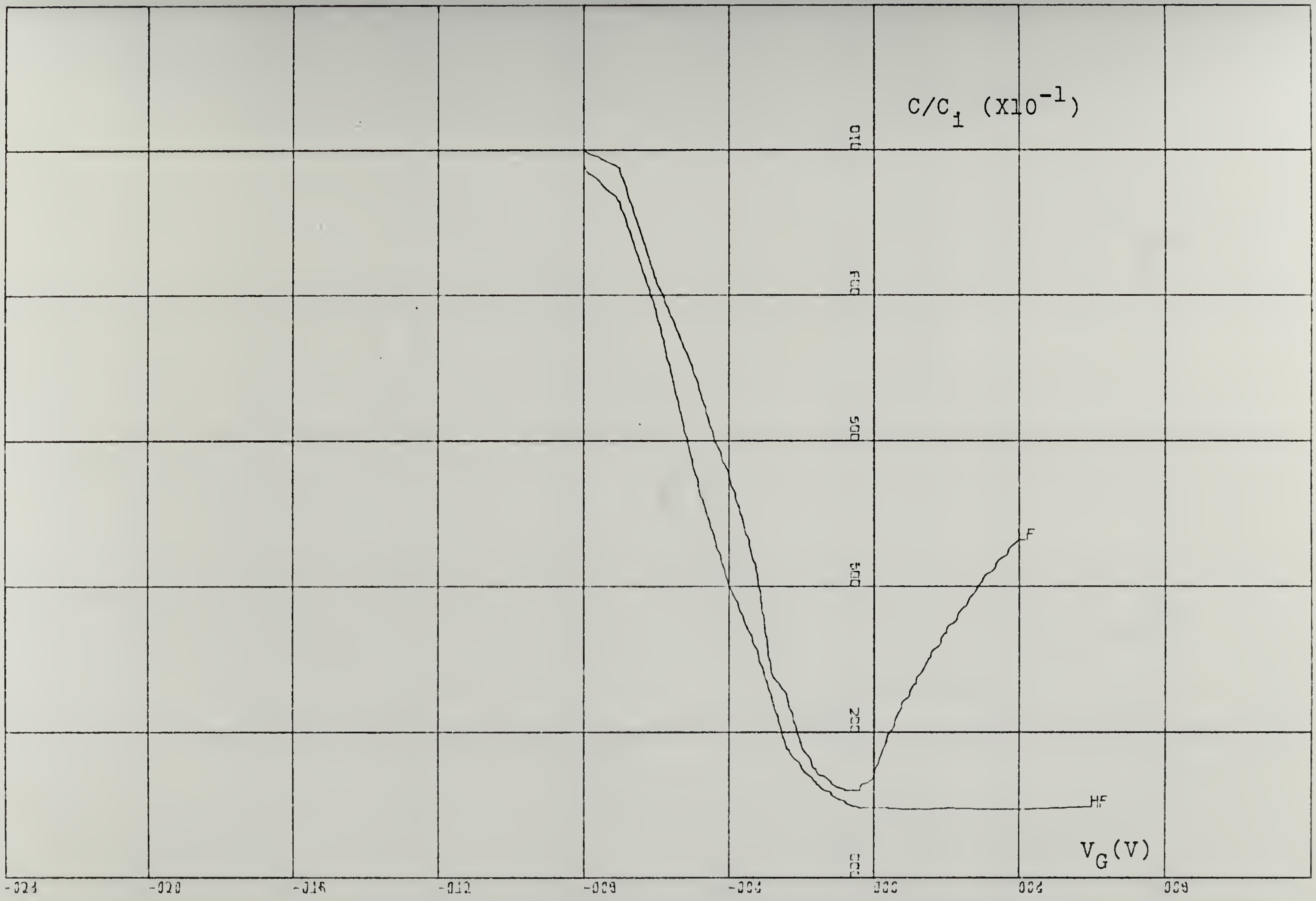

Figure 7-15. Experimental C-V Curves for PbSe MIS #2 Showing Low-Frequency Response, T = 300°K, Insulator: Al_2O_3 (300A°)

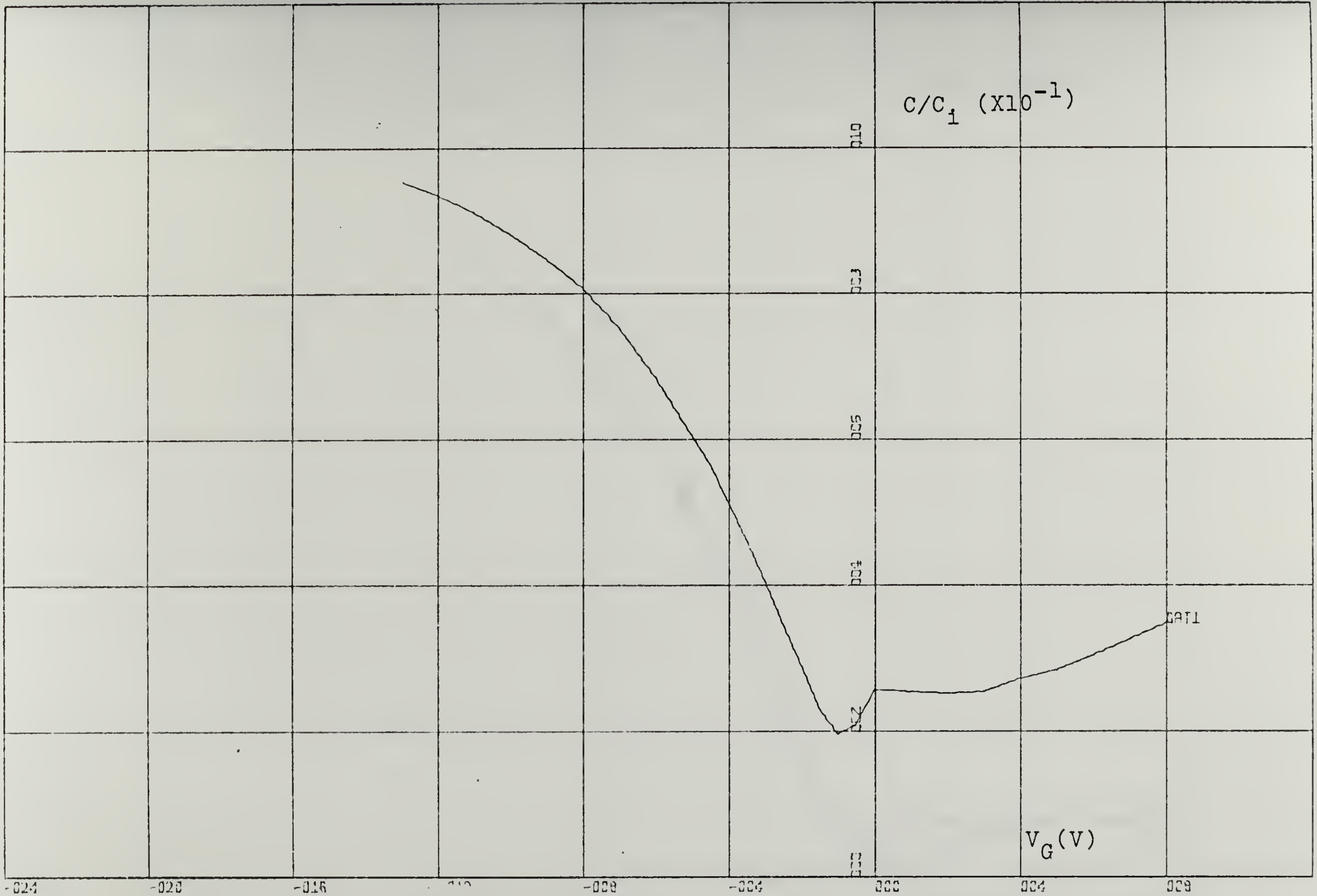

Figure 7-16. Experimental C-V Curve for $Pb_{.97}Sn_{.03}Se$ MIS, T = 300°K, Insulator: Al_2O_3 (300A°)

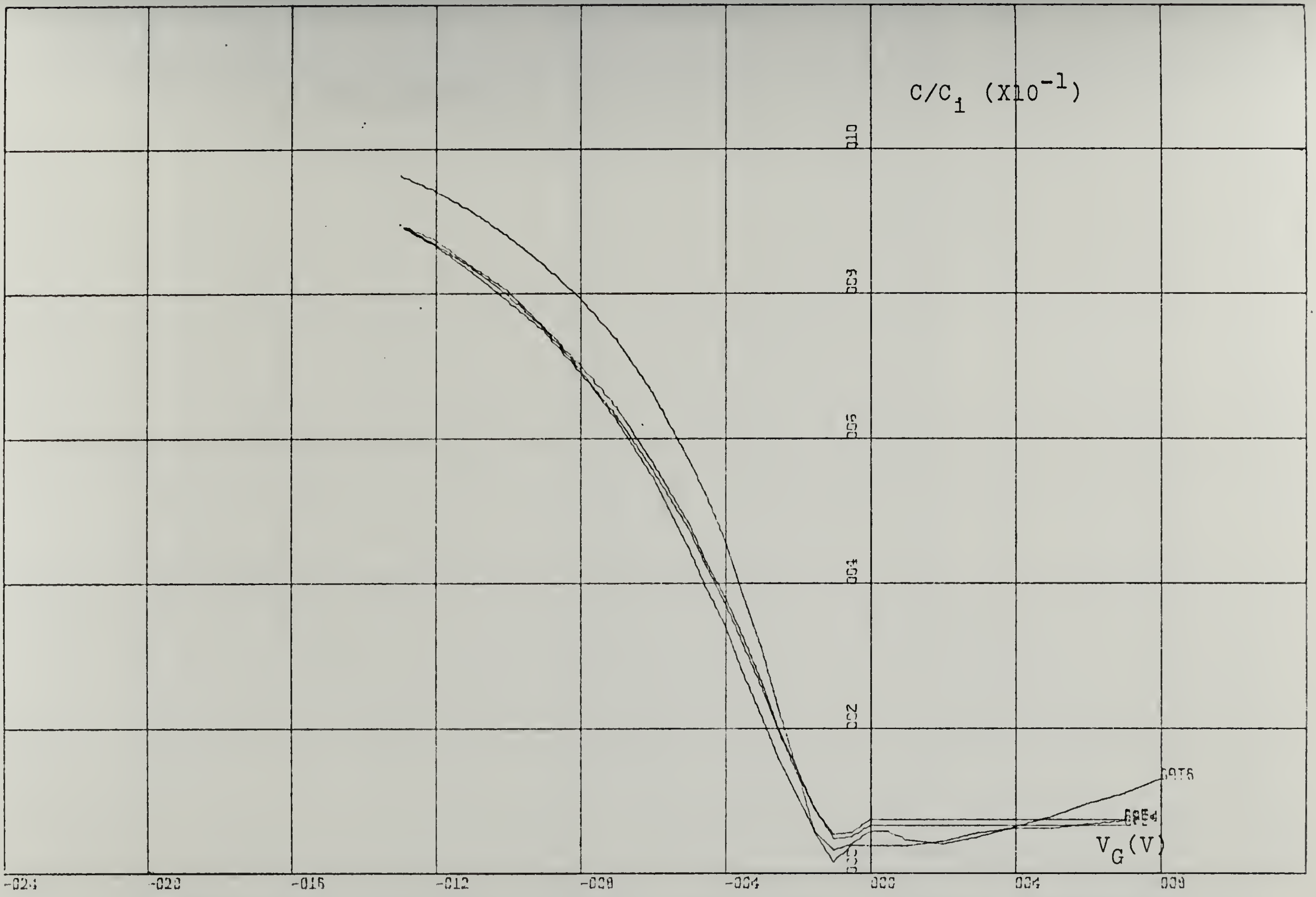

Figure 7-17. Experimental C-V Curves for $Pb_{.90}Sn_{.10}Se$ MIS, T = 300°K, Insulator: SiO_2 (450A°)

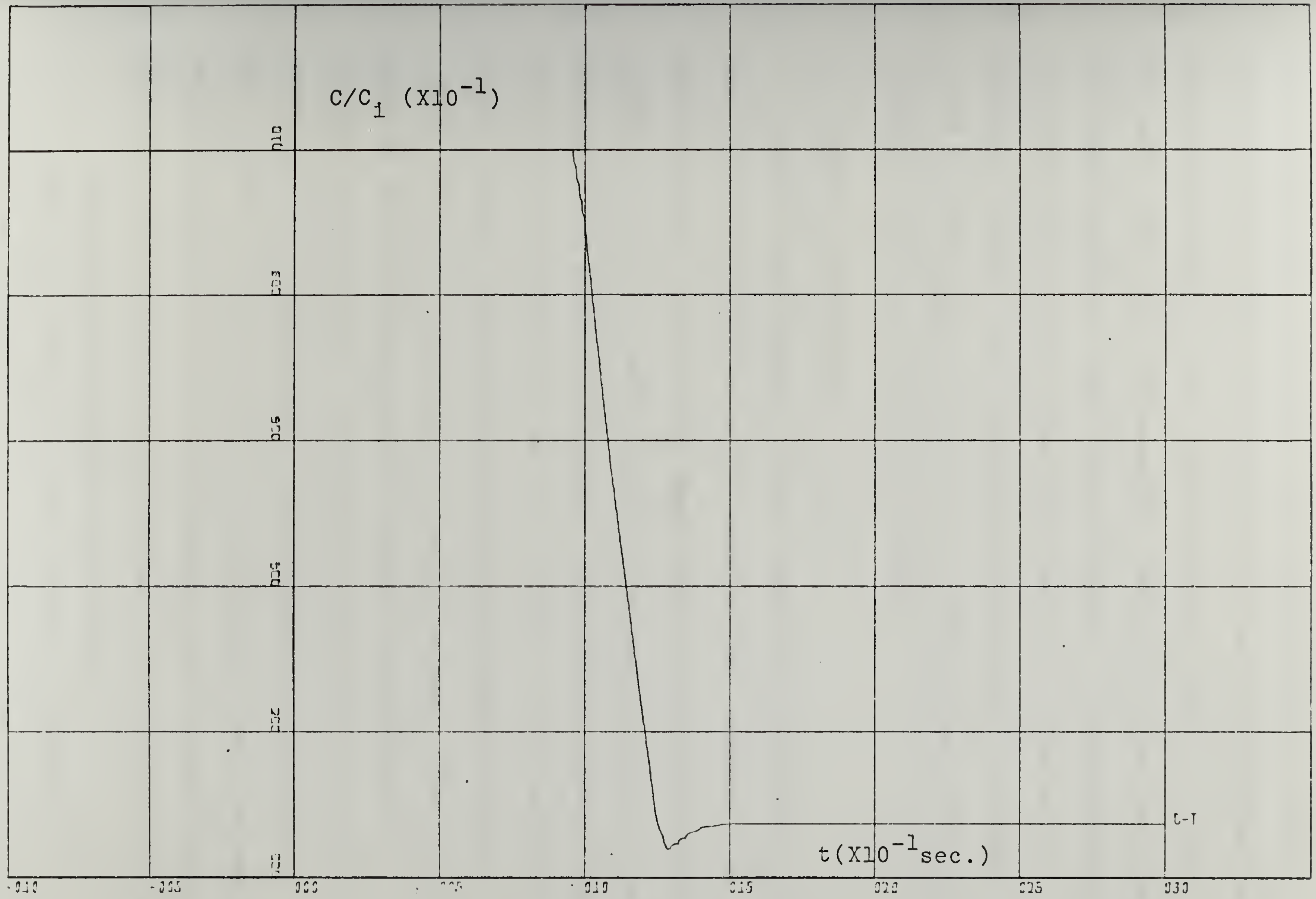

Figure 7-18. C-t Response for Pb$_{.90}$Sn$_{.10}$Se MIS, T = 300°K, Insulator: SiO$_2$ (450A°)

It is clear from the figure that the time for the MIS to relax from the deep depletion to the quasi-equilibrium inversion is about 0.1 sec. This storage time of 0.1 sec. is much longer than the expected time which is on the order of a millisecond or less. The validity of this measurement is questioned; however, the same result was obtained at various different gate locations on the sample. Storage times of this magnitude would allow normal integration and readout times for an IRCCD application.

C. ANALYSIS OF MEASURED C-V DATA

Because low-frequency results were not satisfactory for the lead-tin semiconductor MIS samples, the computer program developed for use with both high and low-frequency C-V curves could not be used except on one sample where a low-frequency C-V curve was obtained. The program based on high-frequency C-V data only, was also tried. It too contained errors because the minimum experimental values of capacitance were much lower than theoretical values. The third part of this section contains computer calculations of minimum high-frequency capacitance versus impurity concentration with insulator type and thickness as parameters. The purpose of this problem is to determine what combinations of MIS parameters of the semiconductor and insulator would lead to a theoretical C-V in better agreement with the measured C-V results.

1. Low and High-Frequency Data Analysis

The data analysis computer program discussed in Chapter V was applied to the C-V curves of the PbSe sample,

Fig. 7-15. Because the curves are distorted from normal C-V variation, it was expected that abnormal behavior would result.

No useful output curves were obtained. The tabular data output appears in Table IV. The impurity concentration does not agree with expected values. For example, the impurity concentration in the bulk (ENB) is less than the intrinsic concentration (about 10^{16} cm^{-3}). The N_{ss} value is about the value expected.

Quantity	Value
ENS	$-1.62X10^{15}$ cm^{-3}
ENB	$-1.37X10^{13}$ cm^{-3}
ϕ_b	-0.189v
N_{ss} (at ψ = -0.083v)	$1.24X10^{12}$ cm^{-2}
N_{ss} (at ψ = 0.0v)	$9.35X10^{11}$ cm^{-2}

Table IV. Summary of Data Analysis Output for PbSe (Al_2O_3-100A°) MIS from Experimental High and Low-Frequency C-V.

2. High-Frequency Only Data Analysis

The high-frequency only data analysis described in Chapter V was applied to the high-frequency curves of four samples: PbTe (SiO_2-450A°), $Pb_{.80}Sn_{.20}Te$ (SiO_2-450A°), $Pb_{.76}Sn_{.24}Te$ (Al_2O_3-100A°), and PbSe (Al_2O_3-300A°). The results of this analysis appear in Table V. Table V shows that the normalized theoretical minimum high-frequency

Sample	Bias (V)	Normalized C_{MINHF}	Surface Potential (ev)	Interface States (cm^{-2})
PbTe	-25.0	0.979	-0.04	$7.01X10^{12}$
	- 5.0		0.00	$2.40X10^{12}$
	0.0		0.19	$8.75X10^{12}$
$Pb_{.80}Sn_{.20}Te$	-15.0	0.962	0.00	$7.19X10^{12}$
	- 5.0		0.00	$2.40X10^{12}$
	0.0		0.10	$2.26X10^{11}$
$Pb_{.76}Sn_{.24}Te$	-15.0	0.736	-0.07	$7.01X10^{13}$
	-10.0		-0.10	$4.84X10^{13}$
	- 5.0		0.00	$2.43X10^{13}$
	- 0.0		0.01	$2.79X10^{11}$
PbSe	-15.0	0.982	-0.03	$9.16X10^{12}$
	- 5.0		0.00	$2.04X10^{13}$
	0.0		0.26	$7.16X10^{12}$

Table V. Summary of High-Frequency Only Data Analysis for Four Lead-Tin Semiconductor MIS Samples.

capacitance is much larger than that obtained experimentally; therefore, errors are expected from this data analysis. For the $Pb_{.76}Sn_{.24}Te$ sample the theoretical minimum capacitances is lower by a considerable amount and more accurate results were obtained. Note that the interface state density in all the samples was about 10^{13} cm^{-2}. This density is 2 to 3 orders of magnitude higher than that obtained from good quality Si-MOS.

3. Theoretical Minimum High-Frequency Capacitance Analysis

Because of the large difference between theoretical and experimental high-frequency minimum capacitances, the program, discussed in Chapter V, was developed to determine what combinations of insulator thickness, insulator type, semiconductor dielectric constant and impurity concentration would lead to better agreement of these capacitance values. Each set of data pertains to a certain insulator type and thickness and the minimum capacitance versus impurity concentration is plotted with the semiconductor dielectric constant as a parameter. The results of this analysis appear in Fig. 7-19 for Al_2O_3 (100A°) and in Fig. 7-20 for TiO_2 (100A°). These two figures represent the closest agreement with the theoretical minimum capacitance. Table VI gives the absolute capacitance minima. Insulator TiO_2 was considered because its high dielectric constant makes it compatable with the lead-tin semiconductor. Table VI indicates that TiO_2 at 1,000A° gives about the same

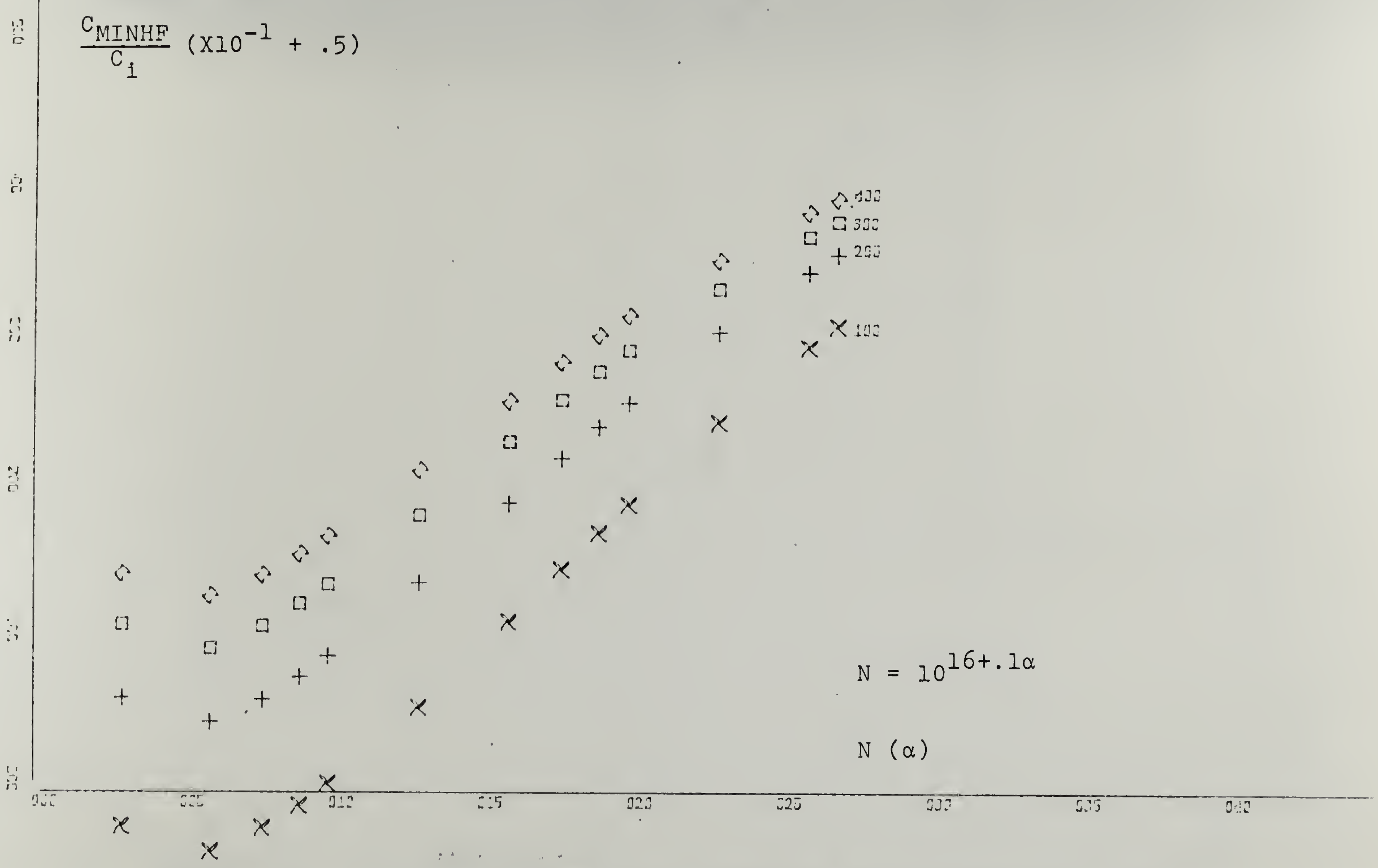

Figure 7-19. Plots of C_{MINHF} Versus Impurity Concentration for IV-VI Semiconductor - Al_2O_3 (100A°) MIS

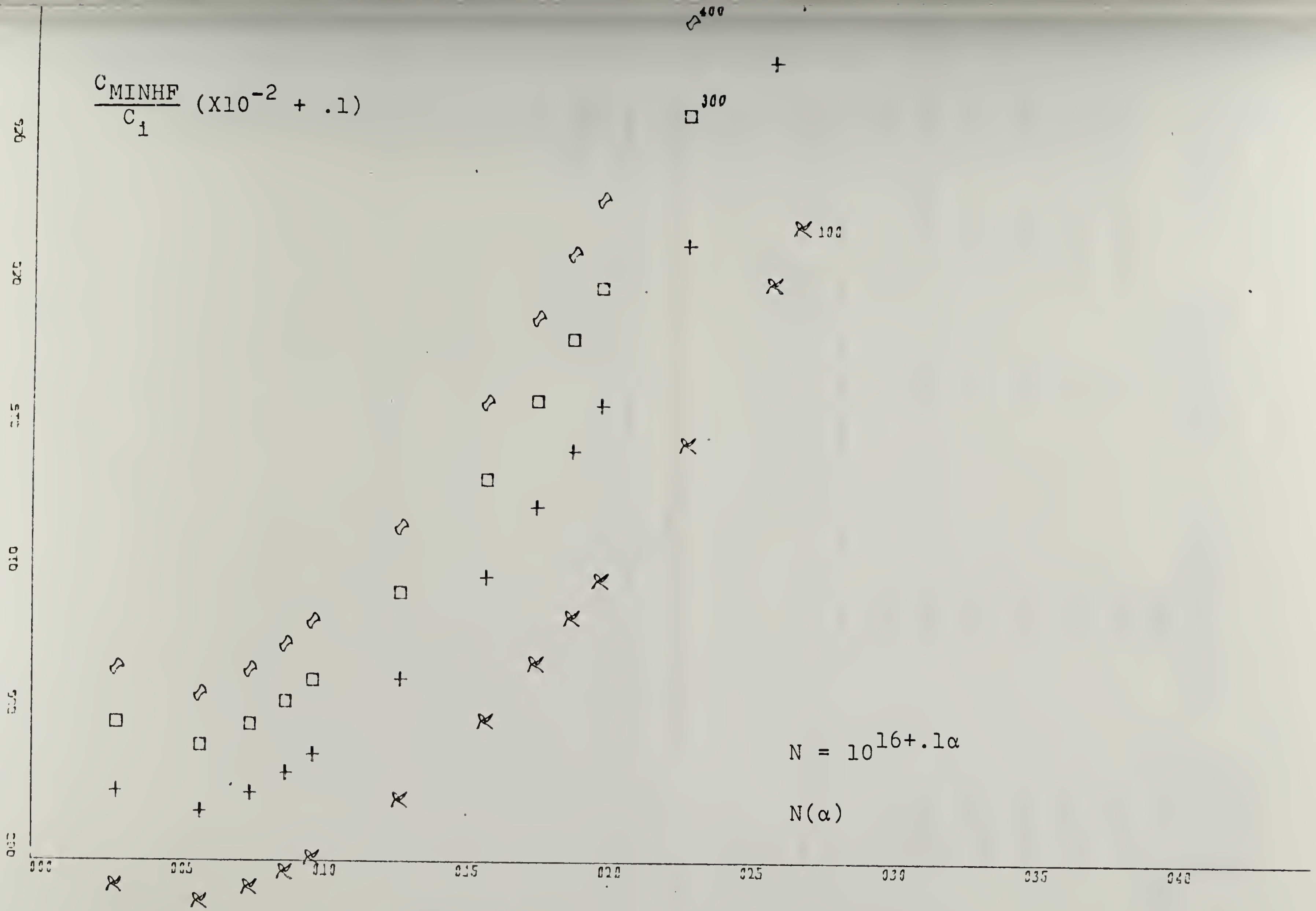

Figure 7-20. Plots of C_{MINHF} Versus Impurity Concentration for IV-VI Semiconductor TiO_2 (100A°)

Insulator Type	Semiconductor Dielectric Constant	Minimum Value of Normalized C_{MINHF}	Impurity Concentration (cm^{-3}) at Minimum C_{MINHF}
Al_2O_3 (100A°)	100	0.461	$4X10^{16}$
Al_2O_3 (300A°)	100	0.720	$4X10^{16}$
SiO_2 (450A°)	100	0.897	$4X10^{16}$
TiO_2 (100A°)	100	0.086	$4X10^{16}$
TiO_2 (500A°)	100	0.320	$4X10^{16}$
TiO_2 (1,000A°)	100	0.488	$4X10^{16}$

Table VI. Summary of Absolute Capacitance Minima for IV-VI Semiconductor MIS

value of minimum capacitance as does 100A° of Al_2O_3. The best fit with experimental minimum capacitance is 100A° TiO_2.

VIII. EXPERIMENTAL RESULTS OF GERMANIUM MIS

Experimental analysis for two different types of Ge-MIS is described in this chapter. To date, almost no research has been done on Ge-MIS. Si-MOS is well established and one doesn't gain much of an advantage from Ge with its energy gap of 0.67 ev., except that its spectral response moves farther toward the infrared. The study of Ge-MIS by the author is a joint effort with Dr. N. Bottka from NWC, China Lake who is doing electro-reflectance research for both basic band structure study and applied tunable IR filter development.

A. DEVICE STRUCTURE

The devices studied were a p-type Ge-MIS with a resistivity of 0.05Ω-cm and an n-type Ge-MIS with a resistivity of 40Ω-cm.[29] The samples were rectangular in shape of dimensions 7 by 17 mm. The p-type sample had 250A° of Al_2O_3 and the n-type had a 180A° of Al_2O_3 as insulator, both deposited by E-gun evaporation techniques at NWC, China Lake. The 3 by 9 mm Ni metal gates were deposited by resistive heating. Copper metal electrodes were epoxyed to both ends of the metal gate and shellac was put over the surface of the gate. These electrodes did not provide satisfactory results for

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[29] These values of resistivity correspond to impurity concentrations of $1.3X10^{17}$ cm^{-3} and $5.0X10^{13}$ cm^{-3} respectively.

MIS studies. On one sample an electrode did not make good contact with the metal gate and no experimental results were possible from it. The metal electrodes on both samples broke and the Hg probe method was finally used.

B. THEORETICAL PROCEDURE

The theoretical procedure for analyzing the Ge-MIS consisted of obtaining first the ideal low-frequency inversion, high-frequency inversion and high-frequency deep depletion ideal C-V curves. These curves were generated by the program developed by Doshier [8]. The calculated C-V curves appear in Fig. 8-1 for n-type Ge-MIS and in Fig. 8-2 for p-type Ge-MIS. The tabular output of the computer program for p-type Ge-MIS appears on page 160.

The p-type Ge-MIS C-V plot is typical of the curves described in Chapter III of this thesis. Q storage is obtained from the difference between the high-frequency inversion and deep depletion capacitance at a certain gate voltage. A typical value at $V_G = 7.53V$, as seen on page 160, is 3.04×10^{12} coul-cm^{-2}, which is comparable to Q storage for Si-MOS. Other quantities shown on page 160 are the depletion and deep depletion depths at various gate voltages, the flat-band capacitance (0.774) and the surface potential at the onset of inversion (0.449V).

The n-type Ge-MIS C-V plot is not typical of the curves described in Chapter III. The primary reason for the difference is due to the low impurity concentration of the

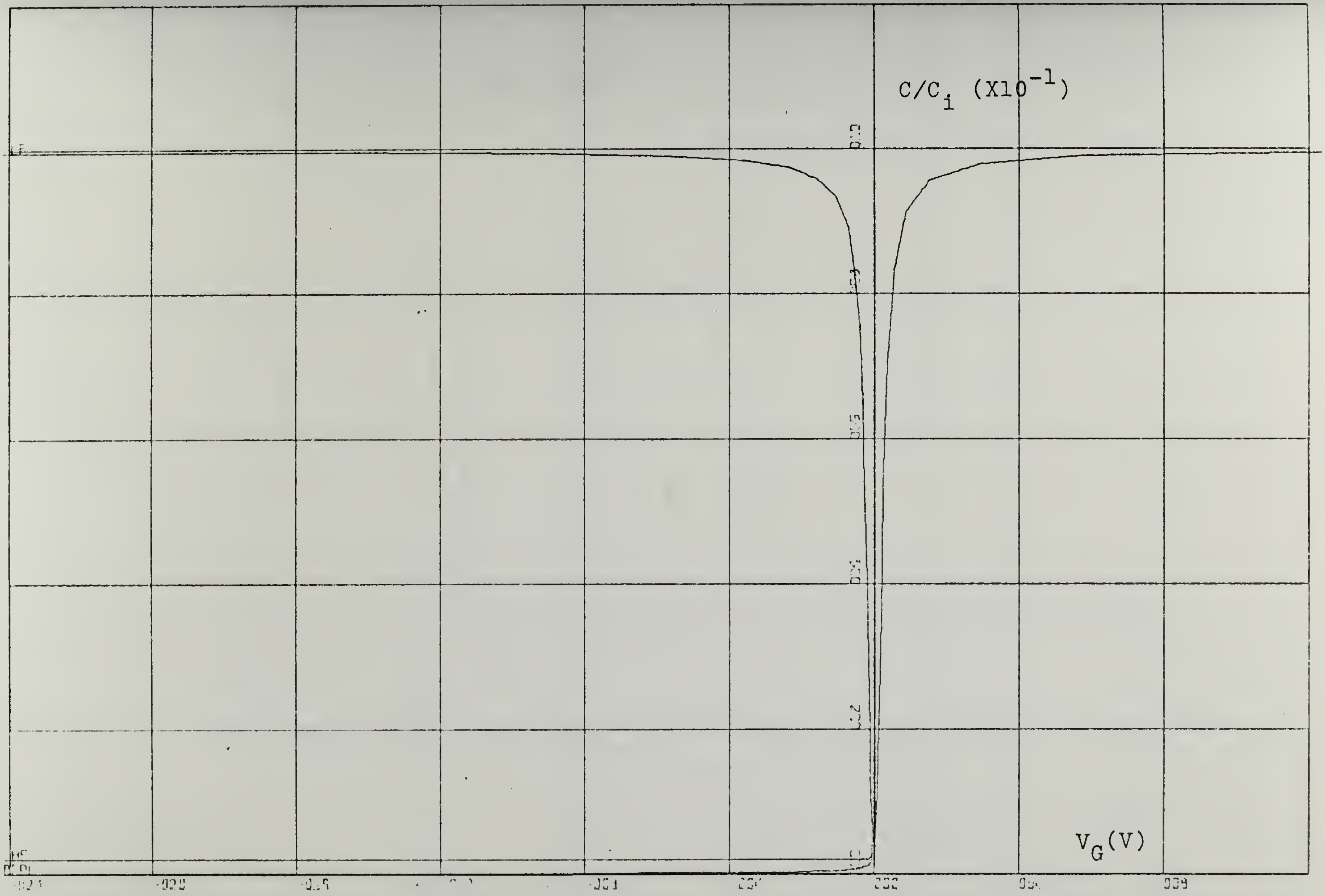

Figure 8-1. Theoretical C-V Curves for n-Type Ge-MIS (Ideal), Insulator: Al$_2$O$_3$ - 180A°, N = 5X10 cm^{-3}, T = 300°K

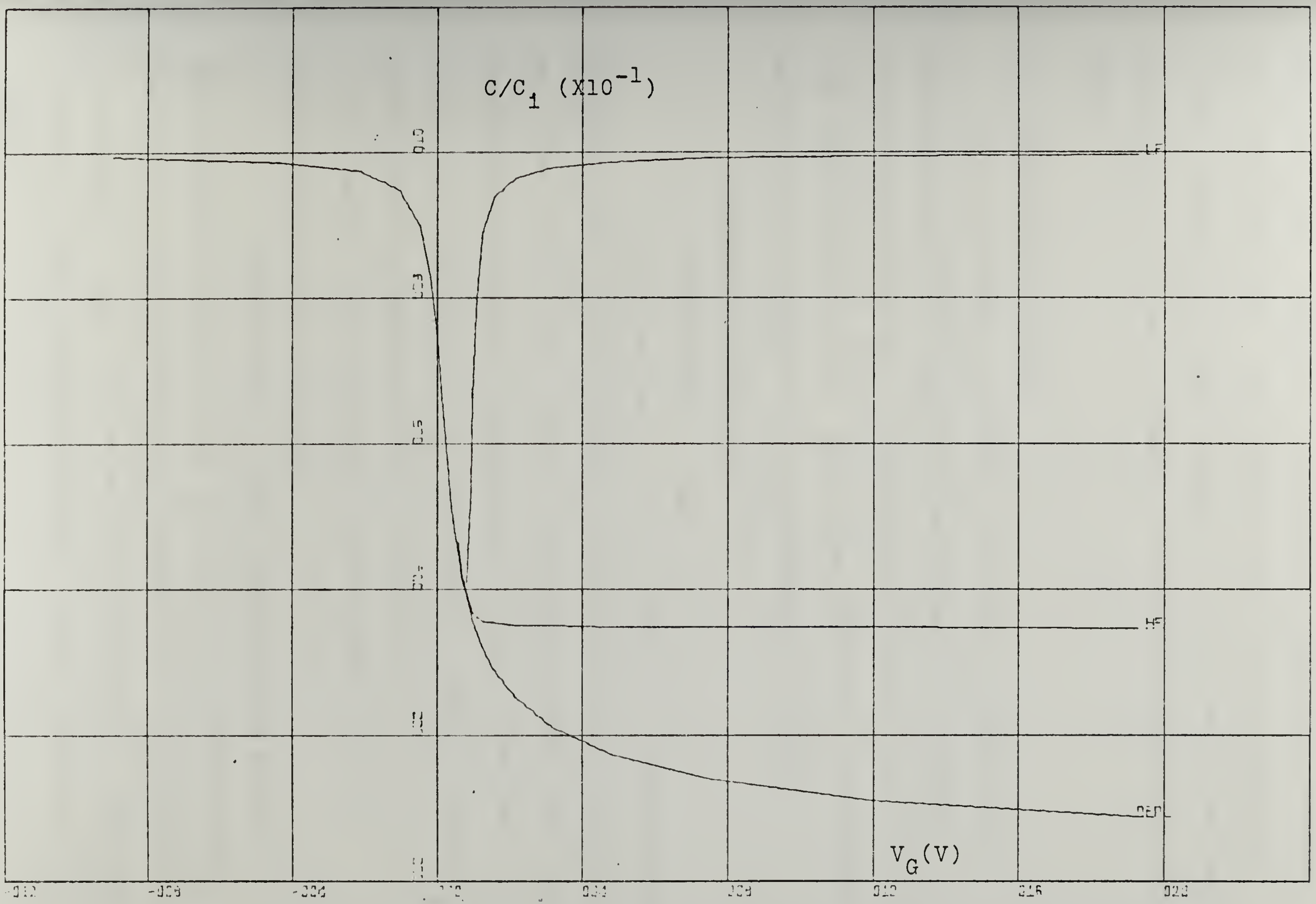

Figure 8-2. Theoretical C-V Curves for p-Type Ge-MIS (Ideal), Insulator: Al_2O_3 - 250A°, N = 1.3X10^{17} cm^{-3} T = 300°K

sample, n_i was $2.2\text{X}10^{14}$ cm^{-3} whereas the impurity concentration was $5\text{X}10^{13}$ cm^{-3}. This sample would not be useful as a CCD. Because its high frequency depletion and inversion capacitances are nearly equal, the storage capacity is very small.

C. EXPERIMENTAL RESULTS

The experimental procedure consisted of three parts: 1) determination of high and low-frequency C-V curves, 2) C-t measurement and 3) the effect of shunt resistance on the experimental curves. This experimentation was conducted as described in Chapter IV on experimental methods.

1. High and Low-Frequency C-V

a. P-type Ge-MIS

The experimental p-type Ge-MIS C-V curves agreed generally with the theoretical curves with three differences as shown in Fig. 8-3. First, a hysteresis effect was found. Second, the measured minimum high-frequency capacitance is larger than the theoretical calculation. Third, the frequency used in measuring the low-frequency C-V is not low enough because the normalized low-frequency inversion capacitance is less than one.

The C-V data of this p-type Ge-MIS sample is not uniform as shown in Fig. 8-4 for three different gate locations. The differences in normalized C are evident. In section D, they will be analyzed separately. Their low-frequency curves are also different but not shown in this figure.

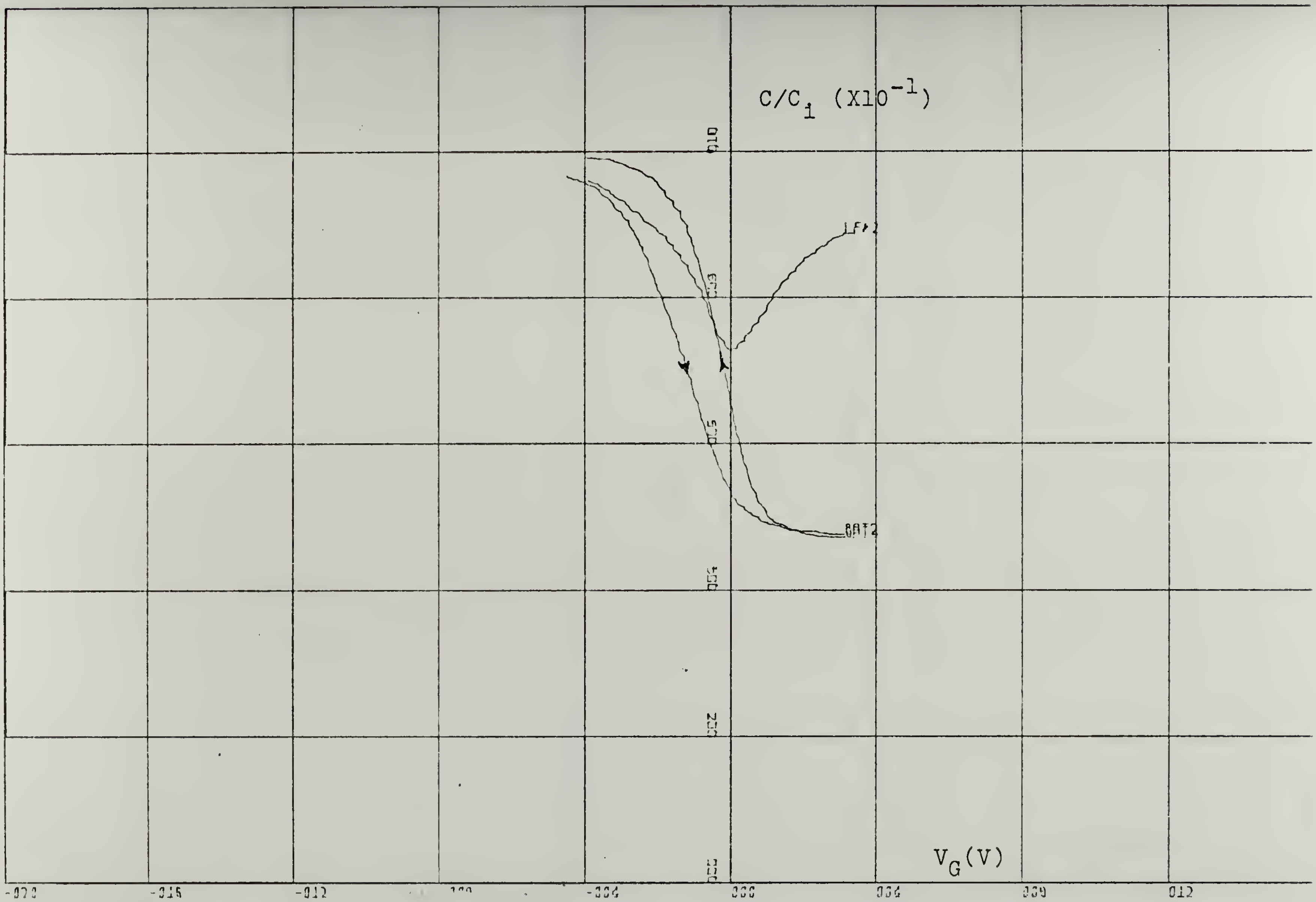

Figure 8-3. Experimental C-V Curves for p-Type Ge-MIS Showing the Hysteresis Effect, Insulator: Al_2O_3 - 250A°, N = $1.3X10^{17}$ cm^{-3}, T = 300°K

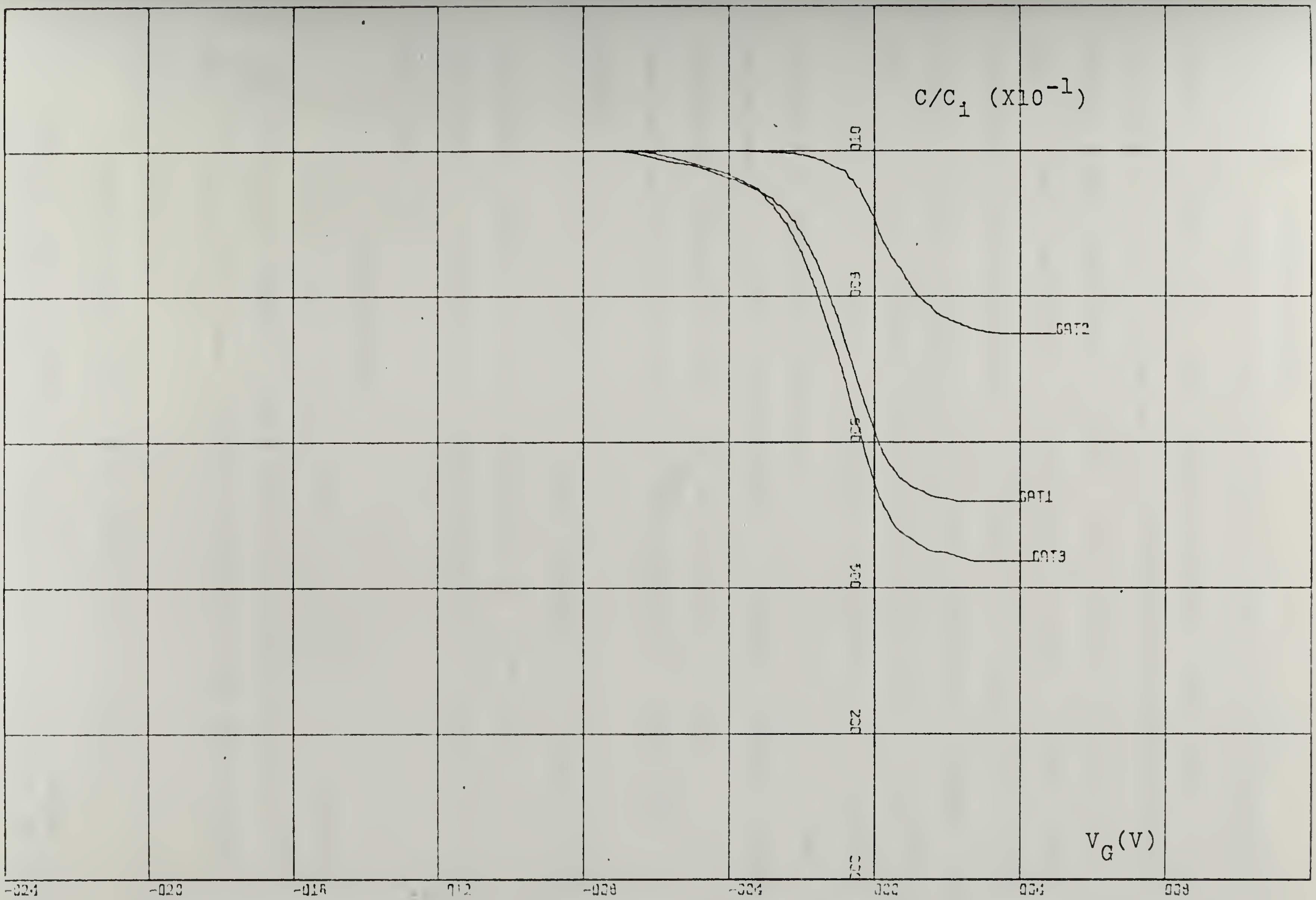

Figure 8-4. Experimental C-V Curves for p-Type Ge-MIS Showing Nonuniformity at Different Gate Locations, Insulator: Al_2O_3 - 250A°, N = $5X10^{13}$ cm^{-3}, T = 300°K

b. N-Type Ge-MIS

Figure 8-5 gives the C-V curves of the n-type Ge-MIS. They differ from the theoretical calculation in two ways. First, the measured inversion capacitances are higher than calculated values. This can be attributed to high contact resistance.[30] Second, the gate voltage range over which the accumulation to inversion capacitance change is much larger. Experimentally this range was between -8.0 and 16.0 volts whereas theoretically this range was between 0.34 and -0.56 volts. A possible explanation of this difference is an over abundance of interface states.[31] The experimental curves are atypical of standard Si-MOS curves. Although hysteresis also exists as shown in Fig. 8-5, it was not as noticeable as the hysteresis for the p-type Ge-MIS.

Since this n-type Ge is almost intrinsic, both the dark current and the generation of minority carriers are small. Consequently, low-frequency C-V variation was not observed.

2. C-t Measurement

Figure 8-6 presents the experimental C-t response of the p-type sample, along with the high-frequency C-V. The voltage pulse was from -8.v to +8.v. The small sharp

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[30] "Finger print" Fig. 3-6b shows this result.

[31] The high-frequency analysis in section D.2 shows about 5 times the interface state density over the p-type Ge-MIS.

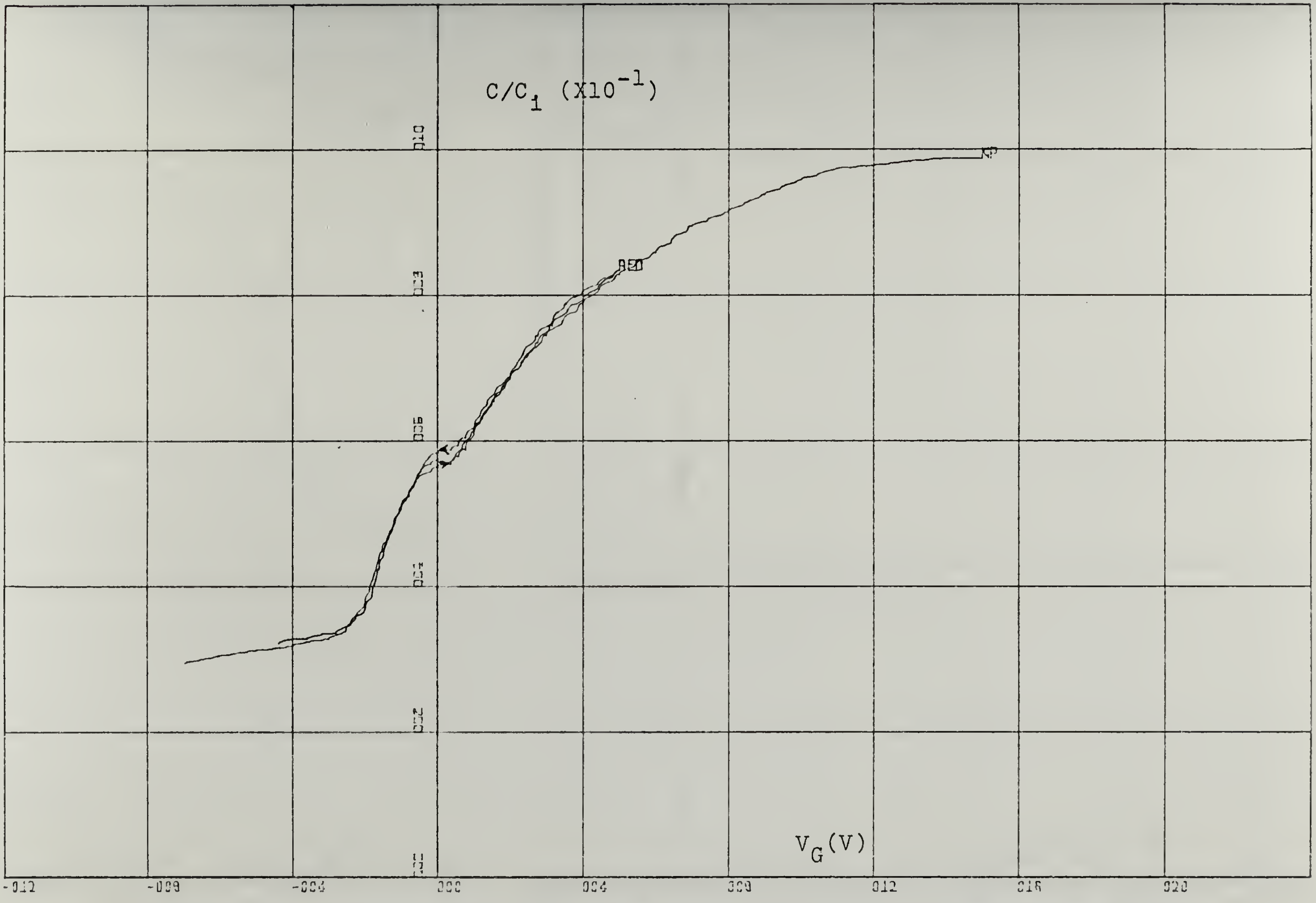

Figure 8-5. Experimental C-V Curves for n-Type Ge-MIS, Red: Reduced Scale Showing Hysteresis, Exp: Expanded Scale, Insulator: Al_2O_3 - 180A°, N = $5X10^{13}$ cm^{-3}, T = 300°K

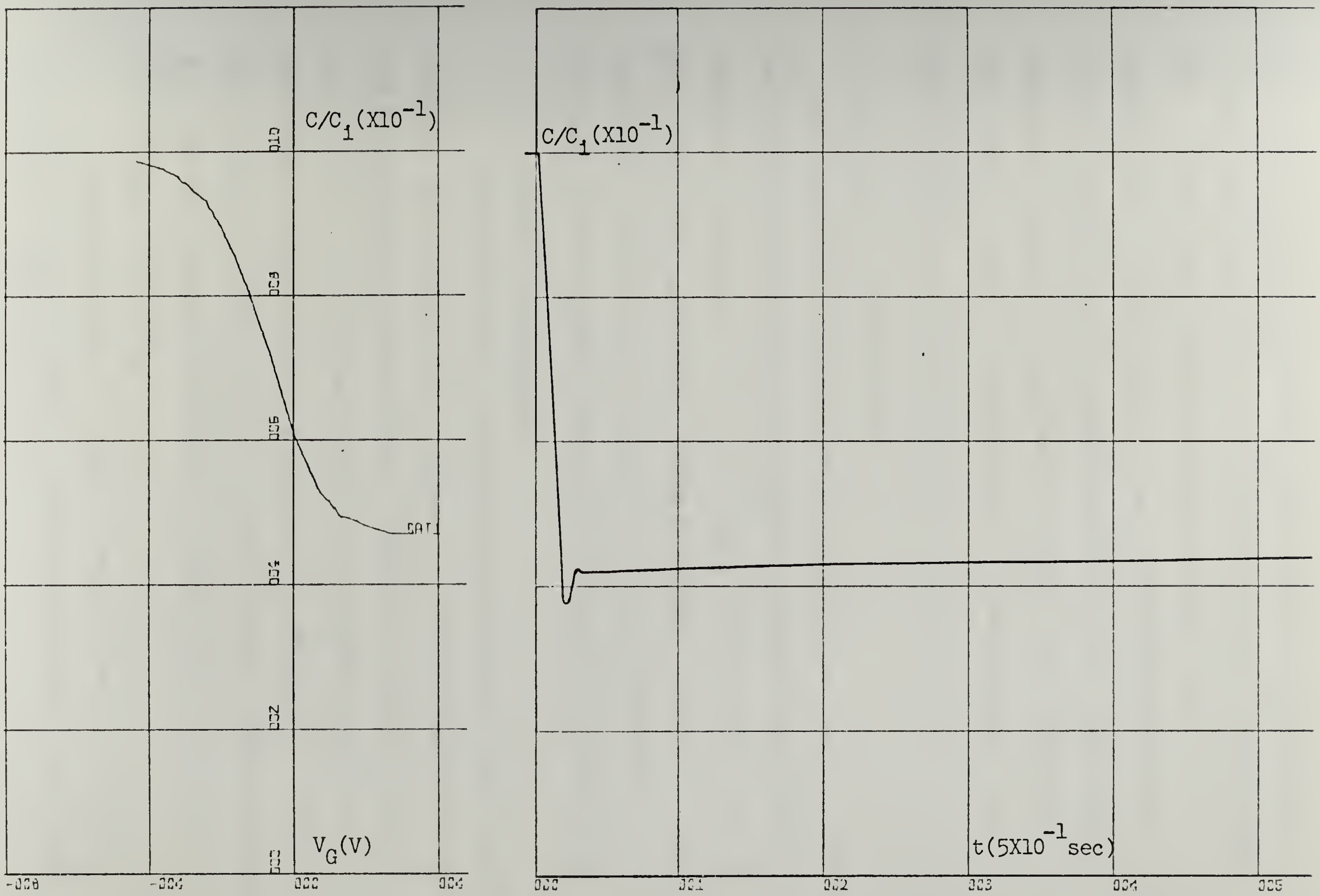

Figure 8-6. Experimental High-Frequency C-V and C-t Response for Ge-MIS (p-Type), a) C-V Response, b) C-t Response

spike at t = 0 sec is probably the result of the filling of fast interface states. The relaxation time (or storage time) is very long as noted by the gradual rise of the capacitance. In this case, it was approximately 60 sec. This is the time for the capacitance to attain the high-frequency inversion capacitance from the deep depletion capacitance. No C-t response could be measured on the n-type Ge-MIS.

D. ANALYSIS OF Ge-MIS DATA

Data analysis consisted of evaluating the low and high-frequency C-V data using the computer program described in Chapter V, section A. For the p-type sample three sets of data, from the same sample, were analyzed. Using the high-frequency C-V, both the p-type and n-type Ge-MIS were analyzed by the program described in Chapter V, section B.

1. P-type Data Analysis

The results for one gate on the p-type Ge-MIS appear in Figs. 8-7 through 8-11. Figure 8-7 is the absolute low and high-frequency C-V curves. Figure 8-8 gives $(C_i/C_S)^2$ as a function U_S together with the straight line fit to the curve. Figure 8-9 is a plot of V_S versus V_a. Figure 8-10 shows the relationship of the interface state density, N_{SS}, and the surface potential. Figure 8-11 provides a plot of Q_{eff} versus V_S.

An examination of these curves reveals that the flat-band voltage, where V_S equals zero in the V_S-V_a plot,

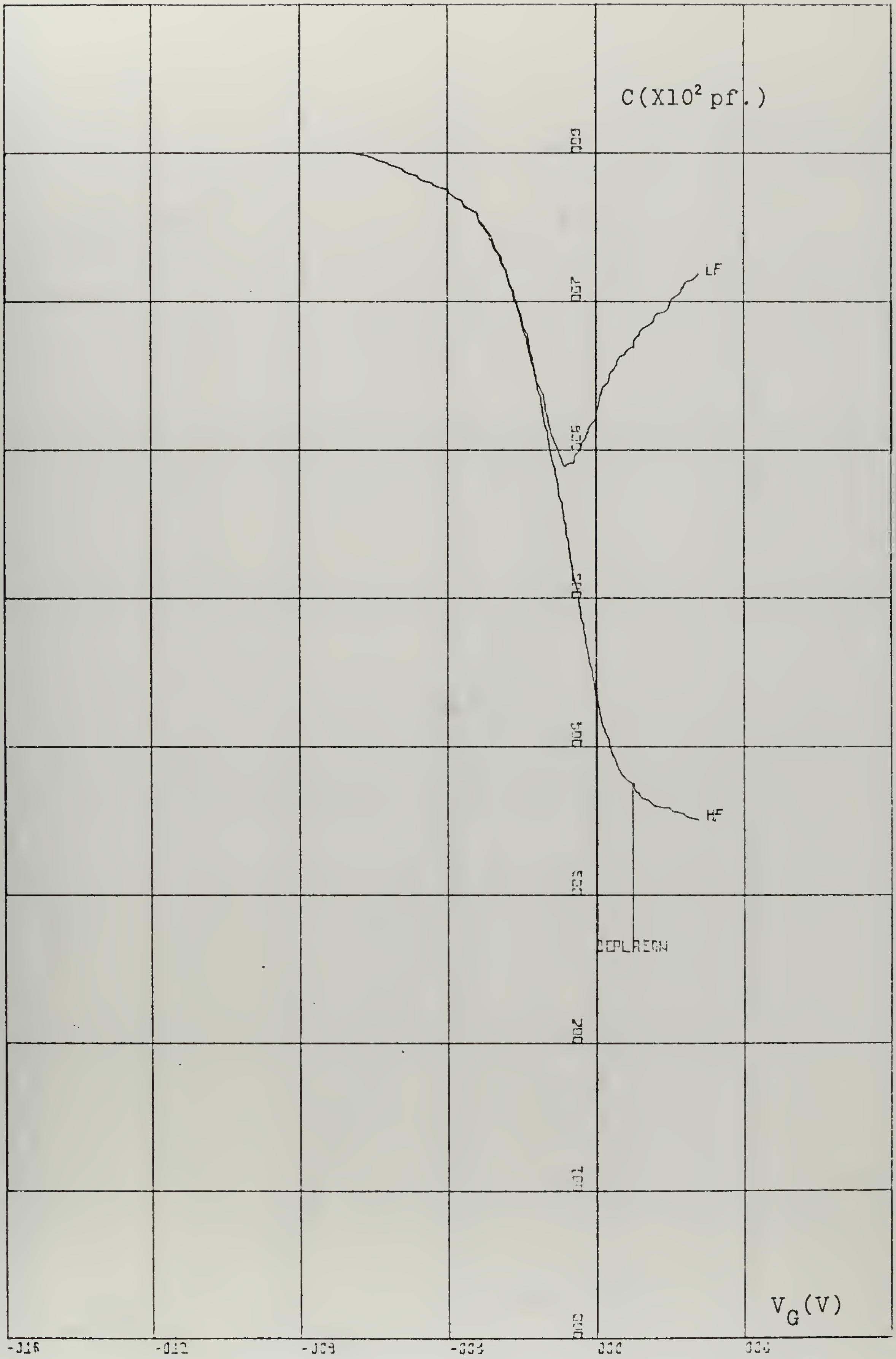

Figure 8-7. Experimental C-V Curves for Ge-MIS (p-Type) Gate #1

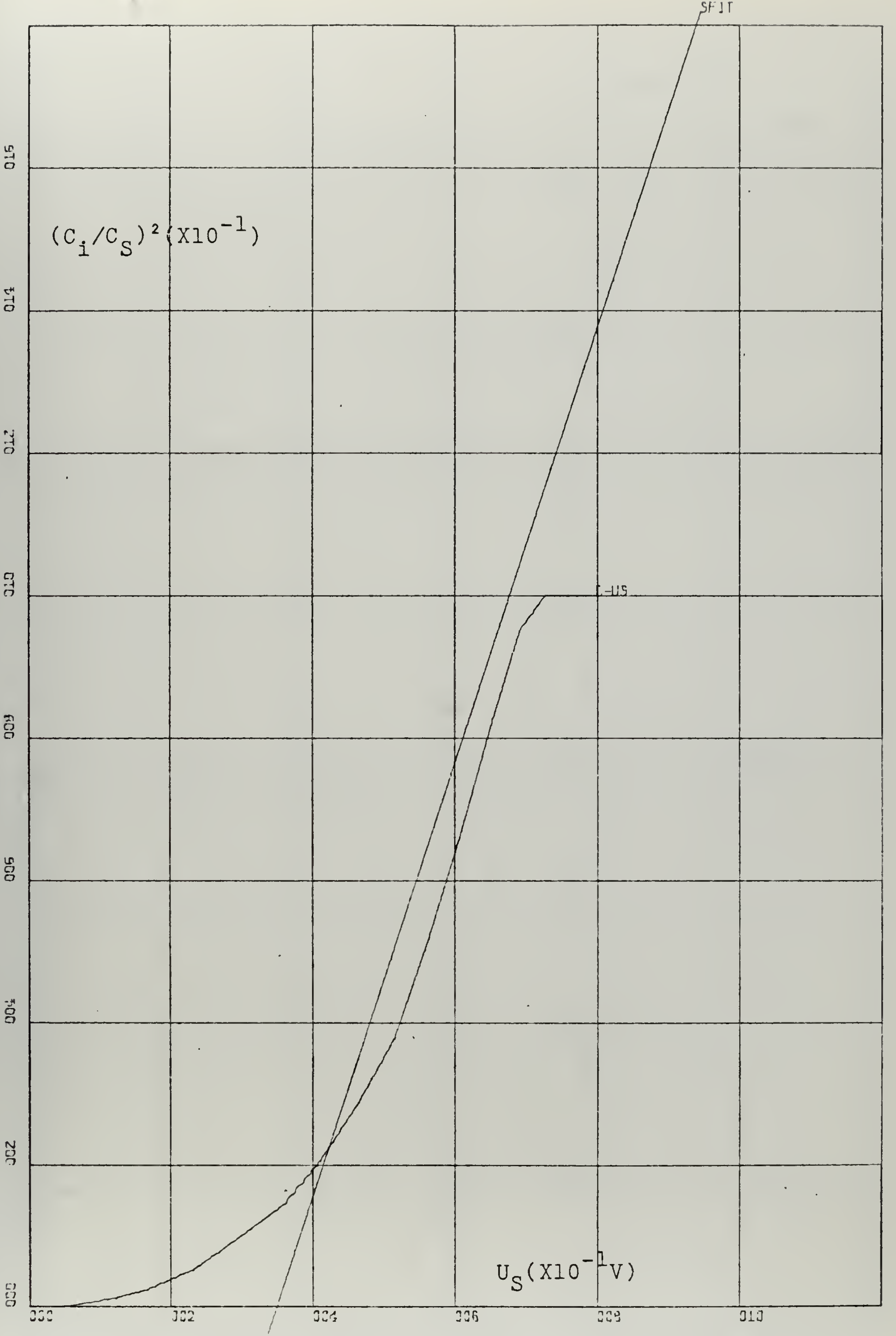

Figure 8-8. $(C_i/C_S)^2 - U_S$ Plot for Ge-MIS (p-Type) Gate #1

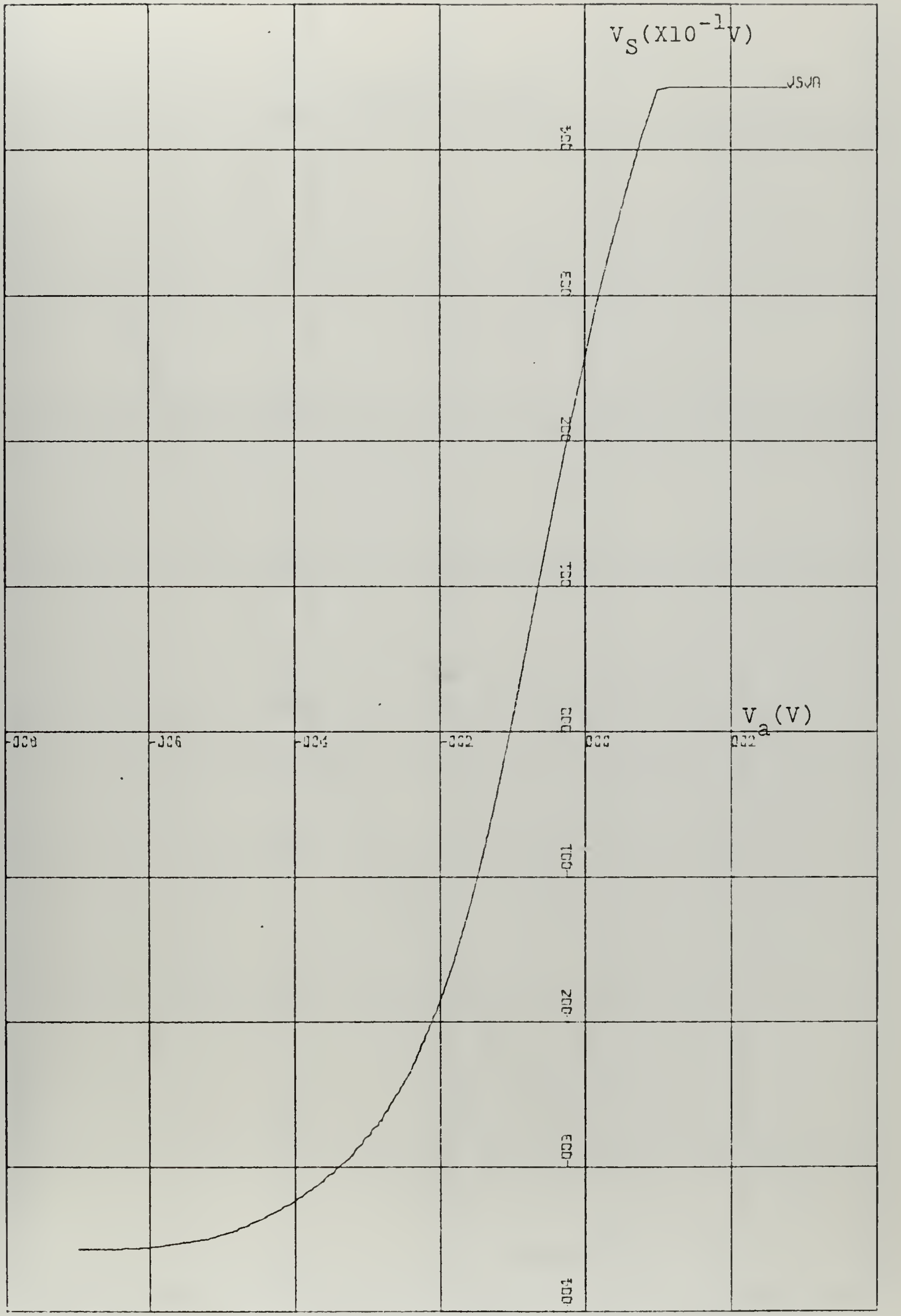

Figure 8-9. V_S-V_a Plot for Ge-MIS (p-Type) Gate #1

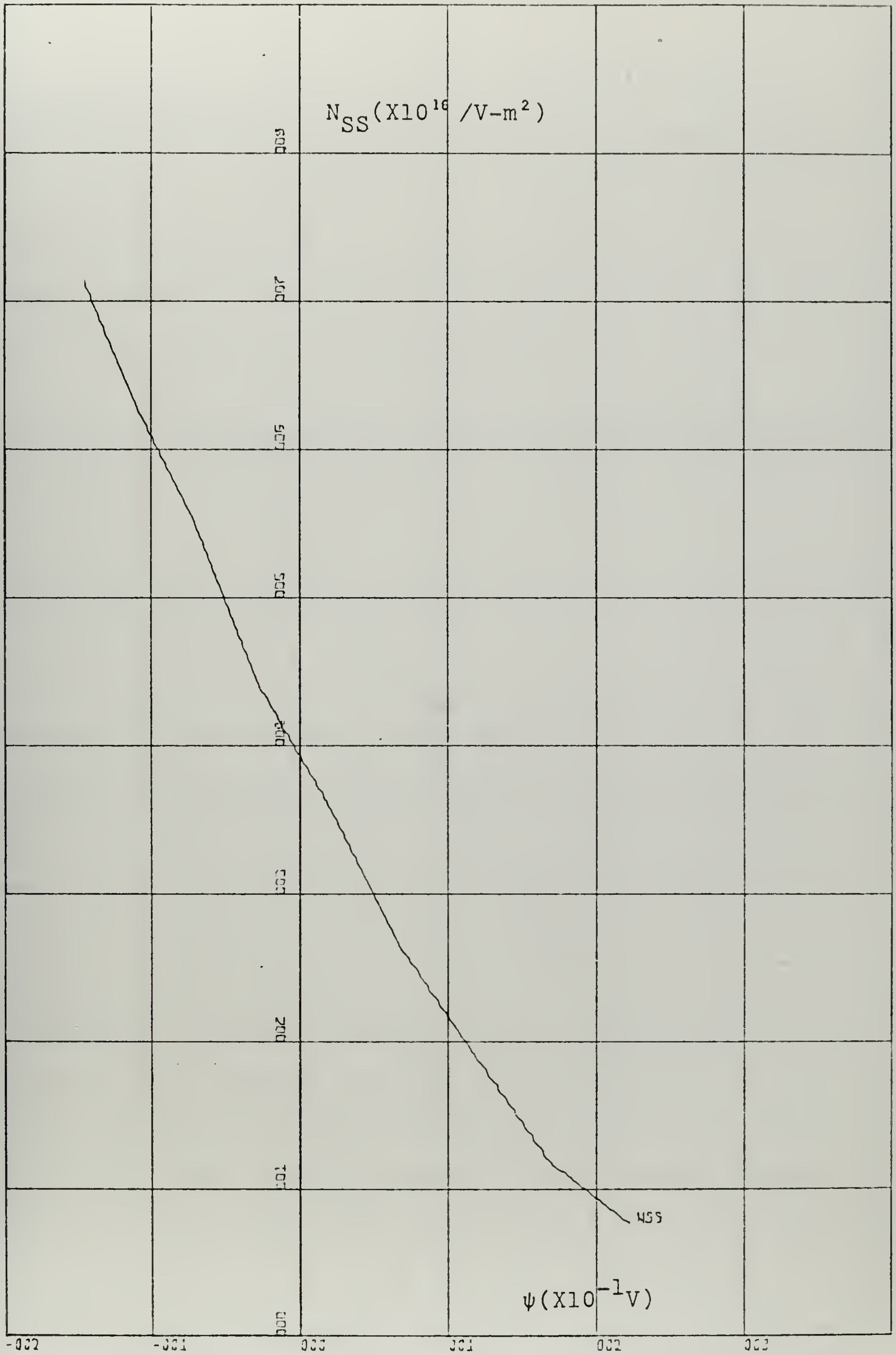

Figure 8-10. N_{SS} - ψ Plot for Ge-MIS (p-Type) Gate #1

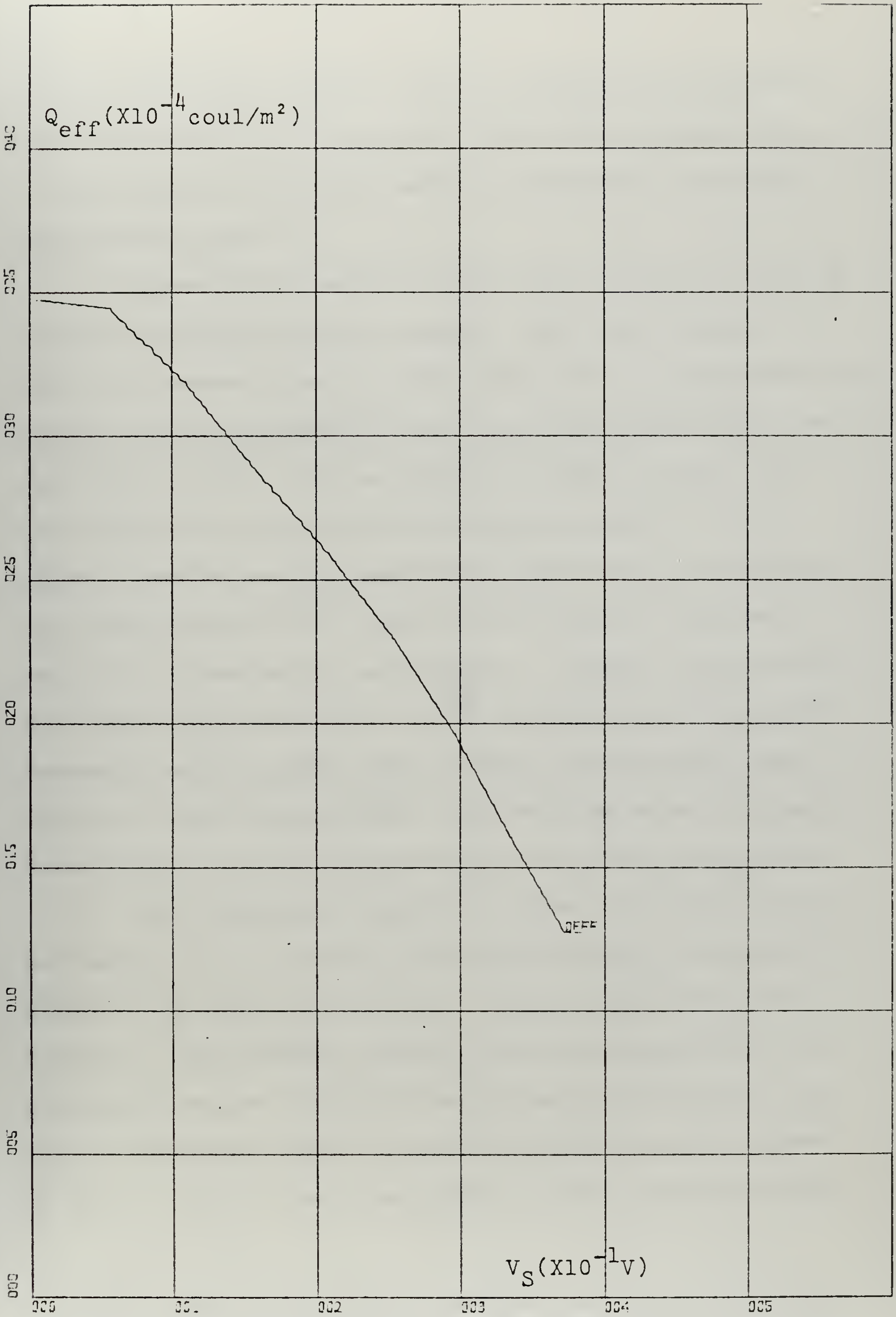

Figure 8-11. $Q_{eff} - V_S$ Plot for Ge-MIS (p-Type) Gate #1

is -1.2 volts and that the range of values of V_S extends from -0.35 volts to +0.45 volts. The total range of V_S is approximately .80 volts which is comparable with the known value of Eg.[32]

Figures 8-12 and 8-13 give the C-V curves taken at two different gates on the sample. The major changes in these two curves from the first gate are: 1) the percentage change between accumulation and inversion capacitance is different (in Fig. 8-7 the change is 66%, in Fig. 8-12 it is 50% and in Fig. 8-13 the change is 30%), 2) the minimum low-frequency capacitance value does not occur at the same voltage on all three curves, and 3) different values of accumulation capacitance. Possible explanations for these differences are nonuniformity in both the semiconductor and insulator and, in the low-frequency case, errors in test measurements. The maximum value of capacitance is due to the different gate areas of the Hg probe.

The differences among the three C-V curves is significant and, as a result, the data analysis curves differ. Figure 8-14 gives the $(C_i/C_S)^2 - U_S$ plot for the gate 3 location. This figure and Fig. 8-8 look similar but are different because of the different scaling present. Two other differences exist between the data analysis curves of gate 3 and the two other gates. These differences are

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[32] For valid results, in equilibrium, the range of V_S should be equal to the value of the energy gap. For Ge Eg = 0.67V.

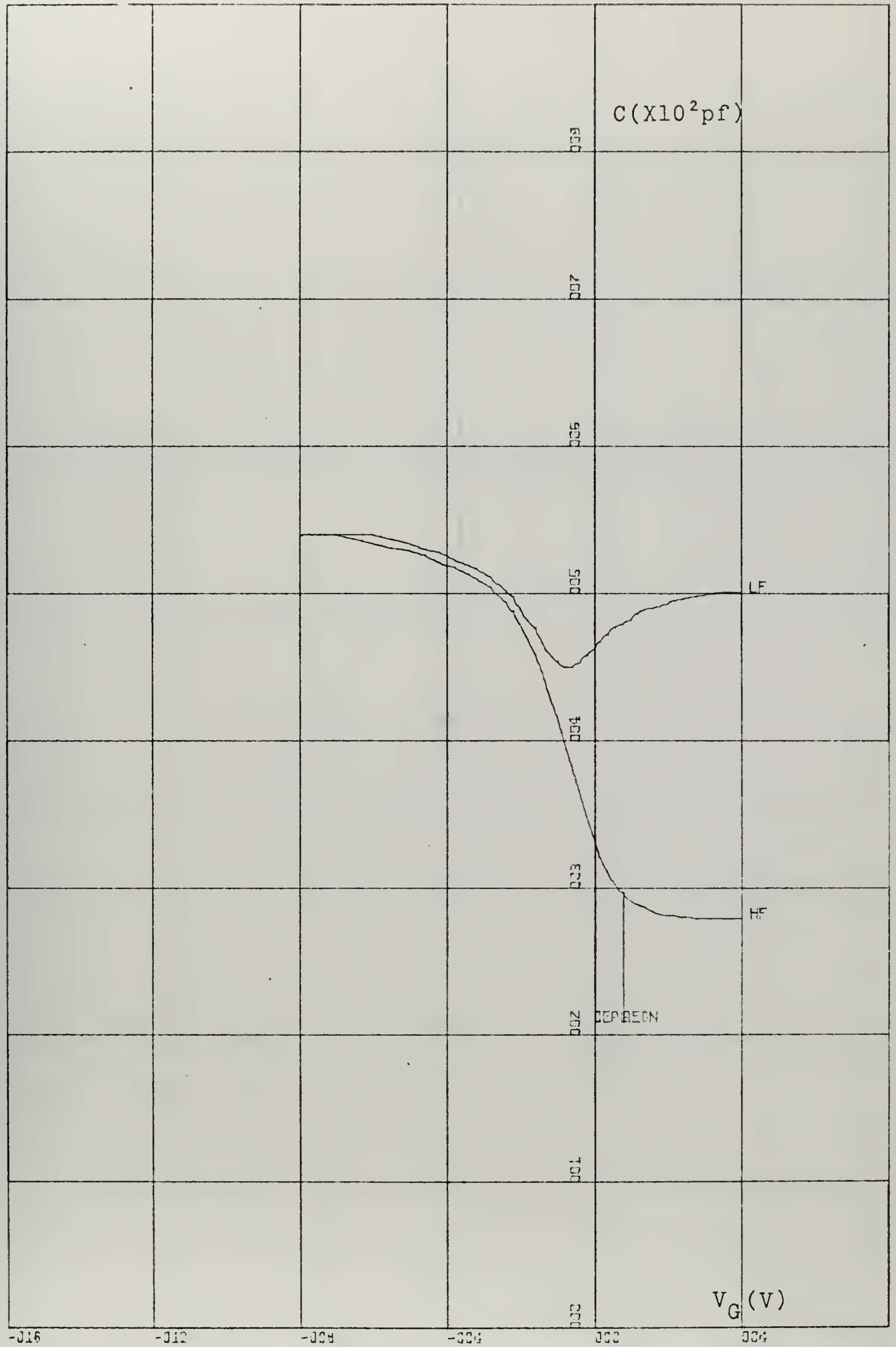

Figure 8-12. Experimental C-V Curves for Ge-MIS (p-Type) Gate #2

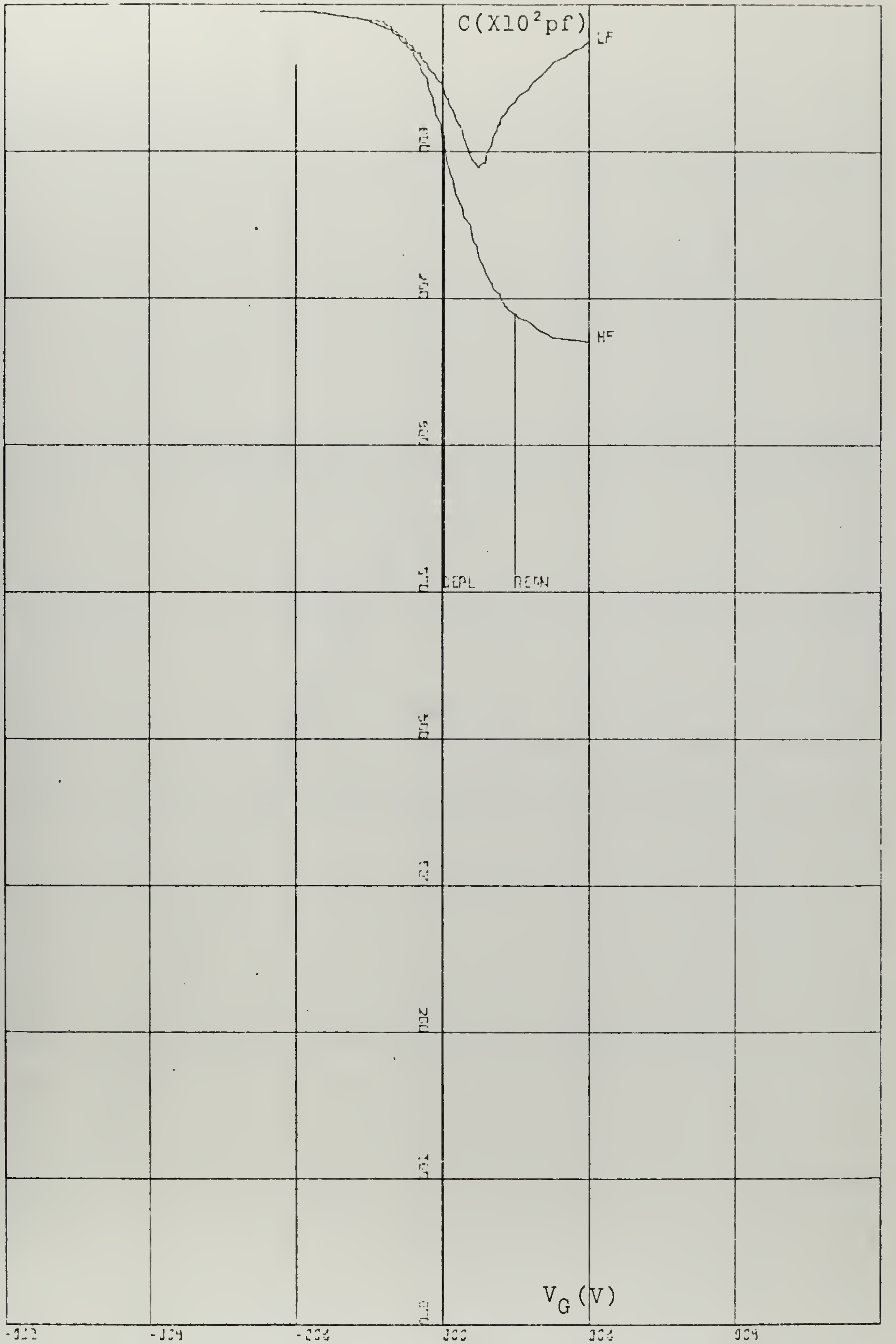

Figure 8-13. Experimental C-V Curves for Ge-MIS (p-Type) Gate #3

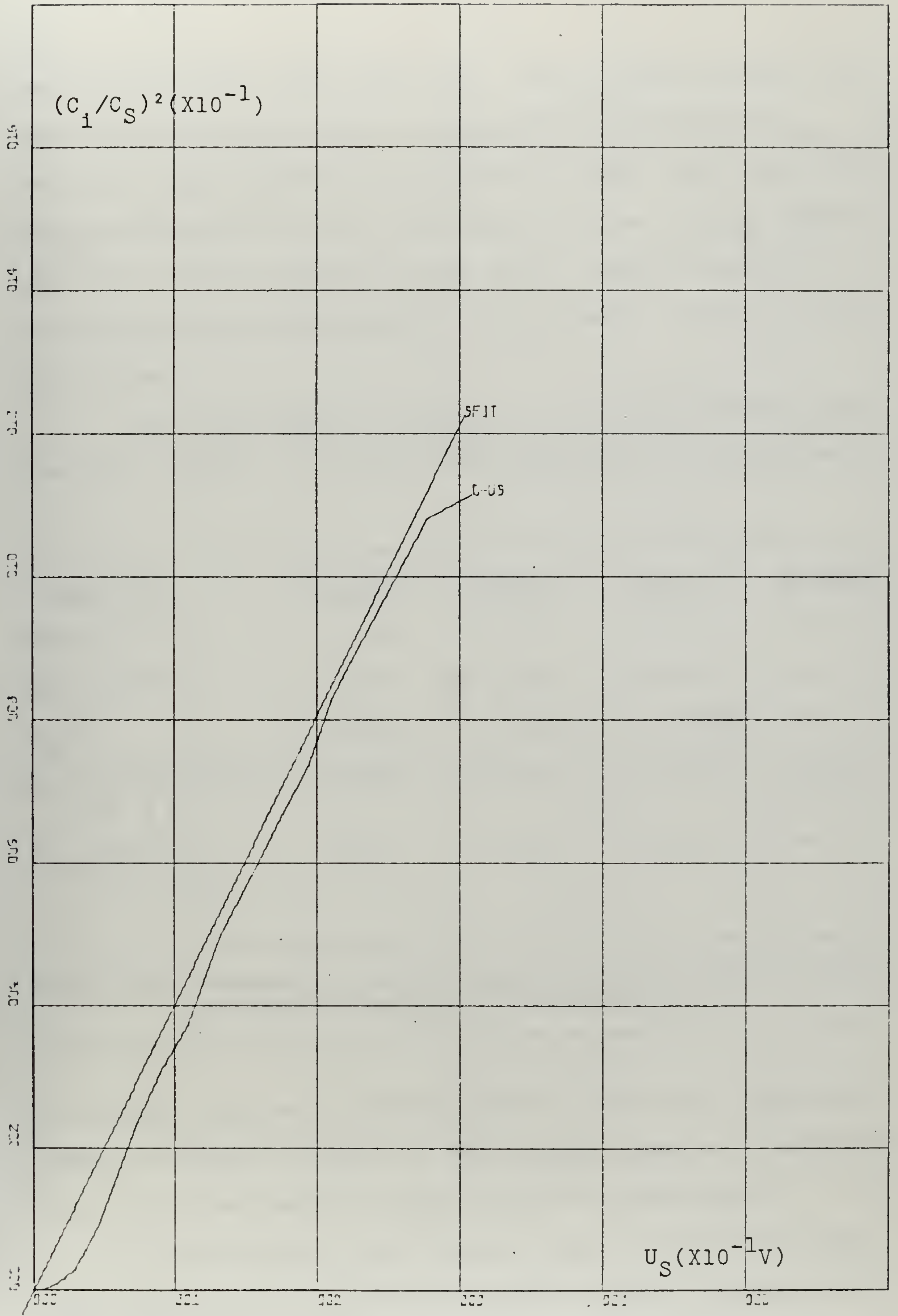

Figure 8-14. $(C_i/C_S)^2$ - U_S Plot for Ge-MIS (p-Type) Gate #3

indicated in Figs. 8-15 and 8-16. The flatband voltage has gone positive with a value of approximately 0.8V and N_{SS} begins to slope upward at a ψ value of .28V. The reason for these differences is due to the shift of the voltage to the right for the C-V curves in Fig. 8-13. Nonuniformities in the insulator and semiconductor are probable causes of these differences.

Table VII gives a listing of the tabular data output from the program. It can be seen from Table VII that there are slight differences between gates 1 and 2 but there is a large difference in gate 3. This again suggests a nonuniformity in the semiconductor and insulator under gate 3.

Quantity	Gate #1	Gate #2	Gate #3	HF Only
ENS($X10^{23}m^{-3}$)	-2.52	-2.98	-19.7	---
ENB($X10^{23}m^{-3}$)	-1.67	-3.56	-36.2	---
ϕ_b(V)	-0.229	-0.248	- 0.308	---
N_{SS}($X10^{16}V^{-1}m^{-2}$) (at ψ = 0)	3.96	13.6	79.3	2.73
N_{eff}($X10^{16}m^{-2}$) (at V_S=0)	2.17	1.71	2.46	---

Table VII. Summary of Tabular Output Data for Three Different Gate Locations on Ge-MIS (p-Type)

The interface state density data obtained from the high-frequency only C-V data analysis is also listed in the

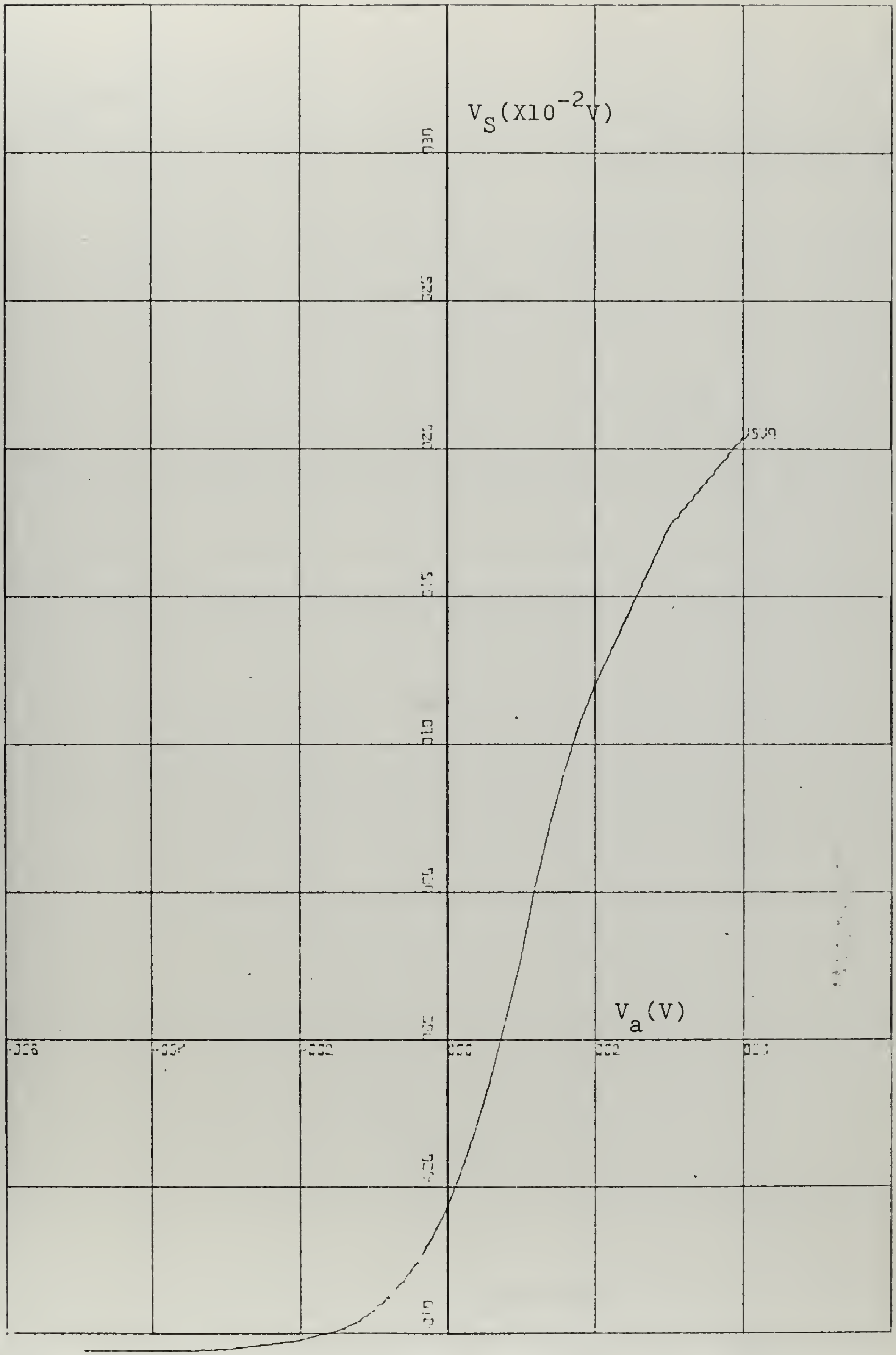

Figure 8-15. V_S-V_a Plot for Ge-MIS (p-Type) Gate #3

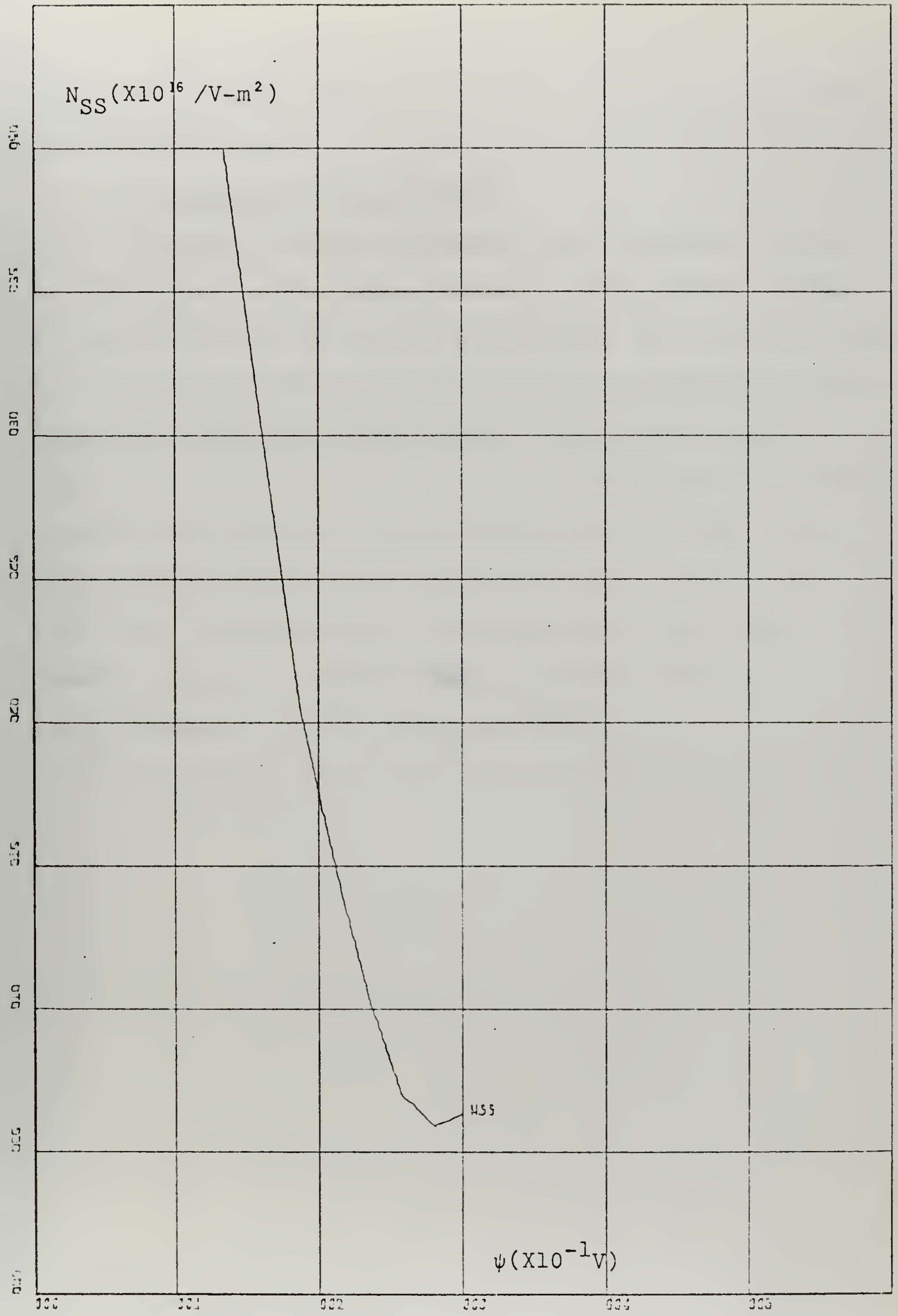

Figure 8-16. N_{SS} - ψ Plot for Ge-MIS (p-Type) Gate #3

table. The density obtained from this analysis agrees with that obtained above.

2. Analysis of n-Type Ge-MIS

Based on the high-frequency only C-V data, results for the n-type Ge-MIS sample appear in Table VIII. Different gate areas led to similar differences as those described for the p-type Ge-MIS sample and will not be presented here. Table VIII shows that the interface state density is 5 times higher than that for the p-type. The theoretical normalized high-frequency minimum capacitance is lower by an order of magnitude than the measured value. Figure 8-5 shows that the experimental high-frequency curve had not reached a minimum. Higher bias voltage was not tried to avoid breakdown of the insulating layer.

Quantity	Value
E_f	0.303 ev
L_d	9.57X10^{-5}cm
C_{MINLF}	0.027
C_{MINHF}	0.021

Bias (V.)	Surface Potential (V.)	Interface State Density (cm^{-2})	Energy Level of States (ev.)
-9.0	0.24	2.50X10^{13}	0.540
-5.0	0.25	1.43X10^{13}	0.550
-1.0	-0.17	2.12X10^{12}	0.130
1.0	-0.19	3.41X10^{12}	0.110
5.0	-0.25	1.48C10^{13}	0.050
10.0	-0.30	2.94X10^{13}	0.003

Table VIII. Summary of Tabular Output Data for Ge-MIS (n-Type)

IX. EFFECT OF ELECTRON BOMBARDMENT ON SILICON N-CHANNEL DEPLETION MOSFET

A. INTRODUCTION

The motivation for this section is twofold. The first factor is to test the computer program described in Chapter VI on a commercially tested standard Si-MOS. The second factor is to investigate the effects of electron bombardment, which simulates the radiation environment around Jupiter [14], on a Si-MOSFET.

B. SAMPLES

Commercial Si N-channel depletion MOSFET's were selected. The I_{dS}-V_{dS} and C-V_G characteristics were measured with a Tektronix type 576 curve tracer and Boonton capacitance meter respectively.[33] The results of these measurements are shown in Figs. 9-1 and 9-2.

C. EFFECT OF ELECTRON BOMBARDMENT

1. Electron Bombardment

The bombardments were conducted at the Naval Postgraduate School Linear Electron Accelerator (LINAC). The energy of the electrons was 64.5 MEV. The electron beam was

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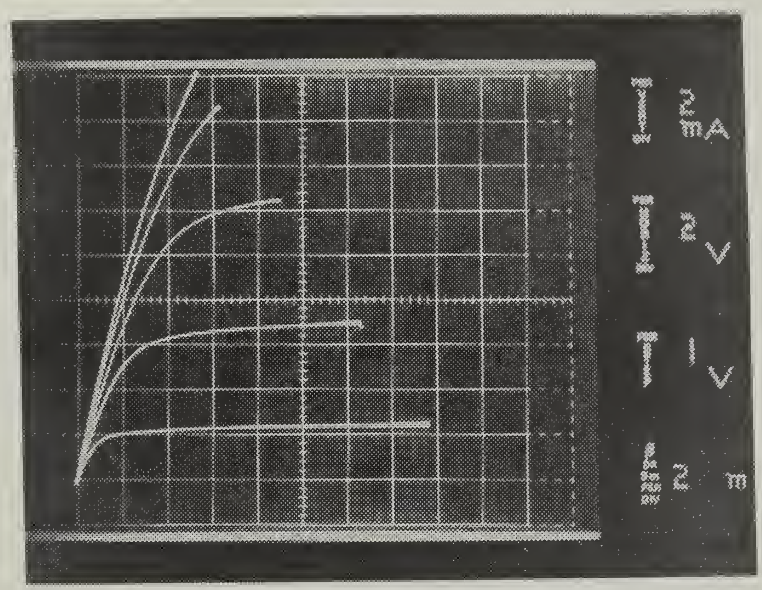
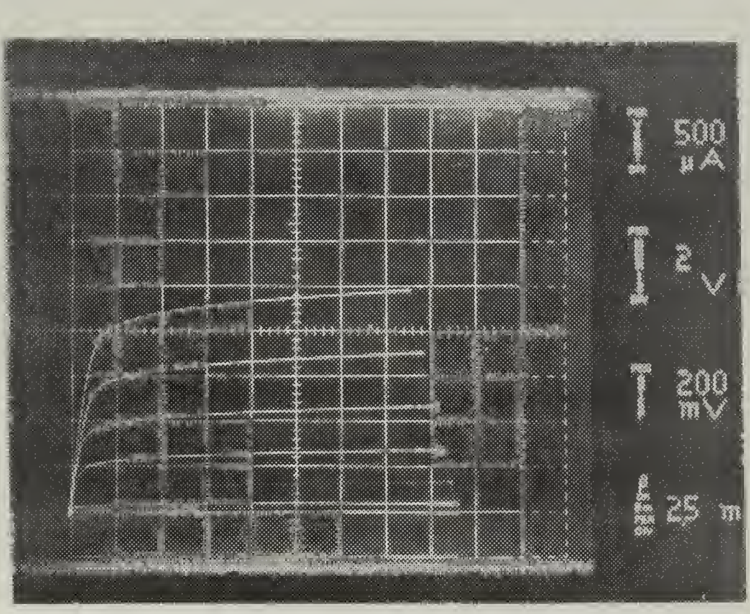
[33] The high-frequency C-V curve was obtained with the source and drain connected to ground, the substrate to the Hi terminal and the gate to the Lo terminal. The low-frequency curve was obtained with the source and substrate to the Hi terminal, the drain open, and the gate to the Lo terminal.



a) Positive Gate Voltage
(bottom most curve: $V_G = 0.V$)



b) Negative Gate Voltage
(topmost curve: $V_G = 0.V$)

Figure 9-1. I_{dS}-V_{dS} Characteristics for MOSFET before Irradiation

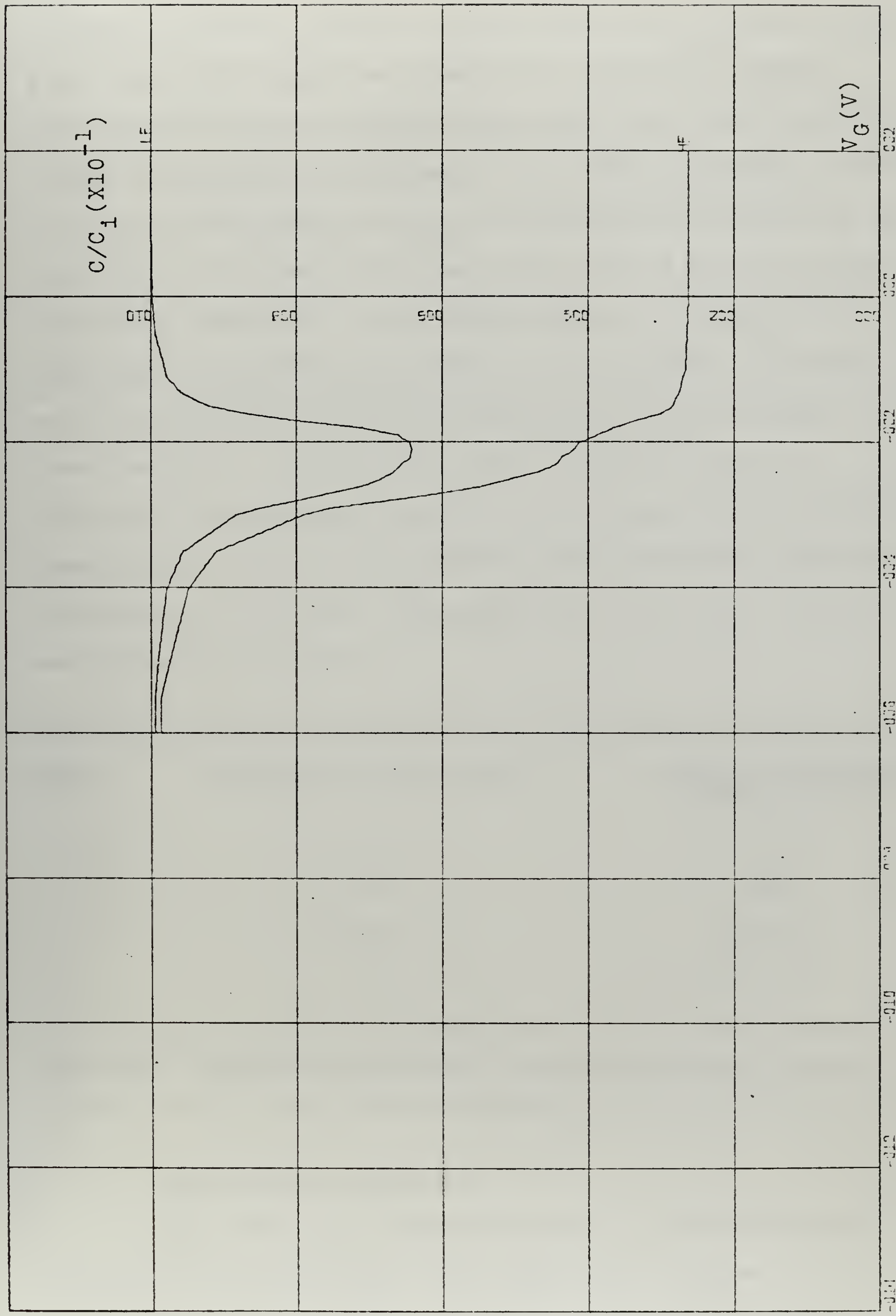


Figure 9-2. C-V Characteristics for MOSFET before Irradiation

focused to provide a nearly circular pattern of approximately 1 cm^2 on a test target as viewed from remote TV cameras. The concentration or electron dosage was determined from the charge accumulated in a Faraday cup. This charge was stored in a .1μ farad capacitor and the concentration found from the equation $N = CV/q$ electrons per cm^2, where V is the voltage across the capacitor. A secondary method to determine the total dose is to time the LINAC "on time" since, by experience, a known dose exists in each pulse for a particular power setting. Electron dose rates from 10^{12} e/cm^2 to 10^{18} e/cm^2 in steps of a power of 10 increase were attempted. These dosages were not realizeable since difficulty was encountered in the LINAC. Table IX gives the actual electron concentration obtained.

Step	Dosage per step (e/cm^2)	Total accumulated dosage (e/cm^2)
1	$1X10^{12}$	$1X10^{12}$
2	$2X10^{12}$	$3X10^{12}$
3	$60X10^{12}$	$6.3X10^{13}$
4	$2.X10^{15}$	$2.063X10^{15}$

Table IX. MOSFET e-Beam Total Accumulated Dosage Obtained

2. Experimental Results

Two electrical characteristics of the MOSFETS were measured before and after the bombardment. These

characteristics are the C-V_G and the I_{dS}-V_{dS}, curves. The pre-bombardment characteristics were given in section B. The MOSFET characteristics after bombardment steps 2, 3, and and 4, are shown in Figs. 9-3 through 9-8. Figures 9-3 through 9-6 give the I_{dS}-V_{dS} characteristics and Figs. 9-6 through 9-8 give the C-V_G characteristics. It is clear from these figures that electron bombardment is, in effect, closing the channel. For each electron dose step the drain-to-source current is lowered, for a certain gate voltage, and the valley of the low-frequency C-V curves widens. A second MOSFET was also tested with the first. The results for it are similar and will not be presented in this thesis.

3. Experimental Analysis

Two types of analysis were made. First the effect of electron bombardment on the threshold voltage, V_{th},[34] of the MOSFET was obtained from the I_{dS}-V_{dS} characteristics. It was found that the V_{th} was shifted to the right after electron bombardment. The shift of V_{th} as a function of electron dosage is shown in Table X.

Second, the physical changes of the device are presented by determining the change of parameters of the MOS structure. These parameters are: 1) ϕ_S-V_G, the surface potential and gate voltage relation, 2) N_{SS}, the interface

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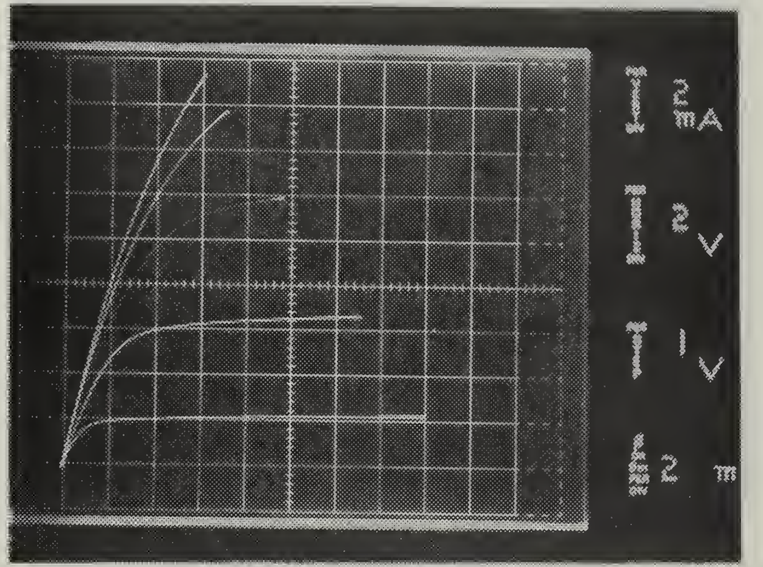
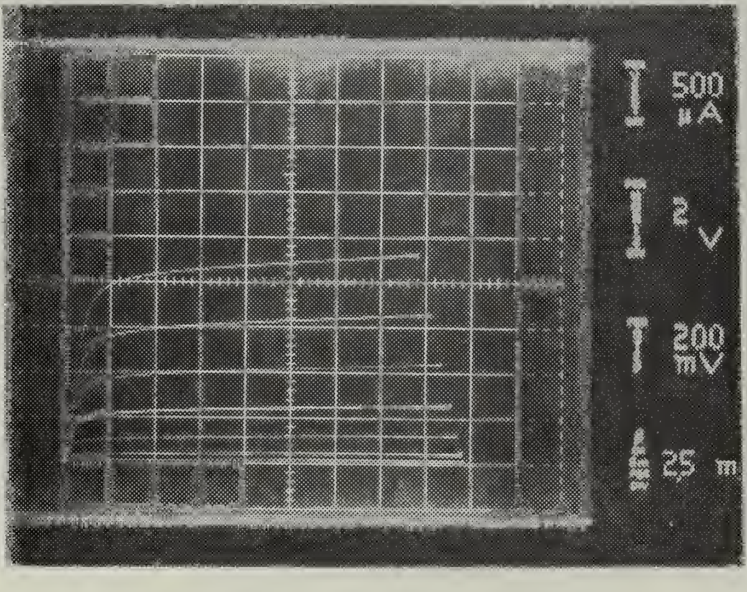
[34] V_{th} is the gate voltage at which the MOSFET begins to conduct.



a) Positive Gate Voltage
(bottom most curve: $V_G = 0.V$)



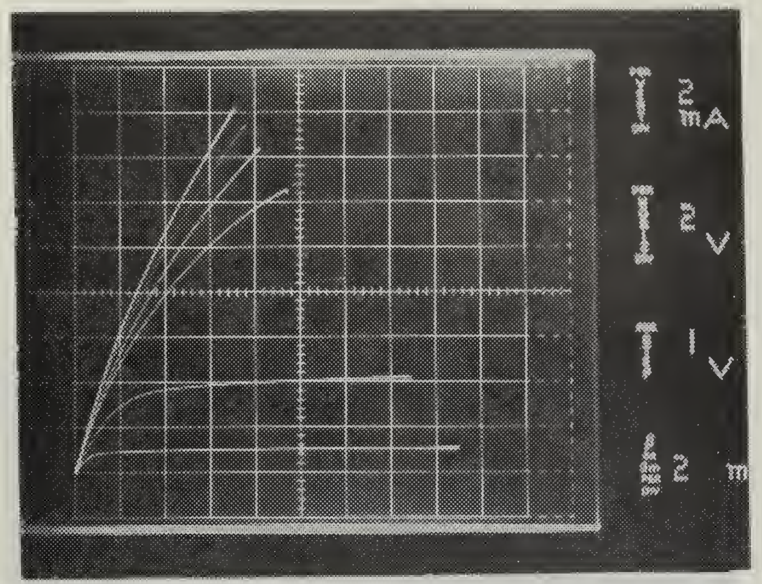
b) Negative Gate Voltage
(topmost curve: $V_G = 0.V$)

Figure 9-3. MOSFET I_{dS}-V_{dS} Characteristics after a Total Accumulated Dosage of $3X10^{12}$ e/cm^2

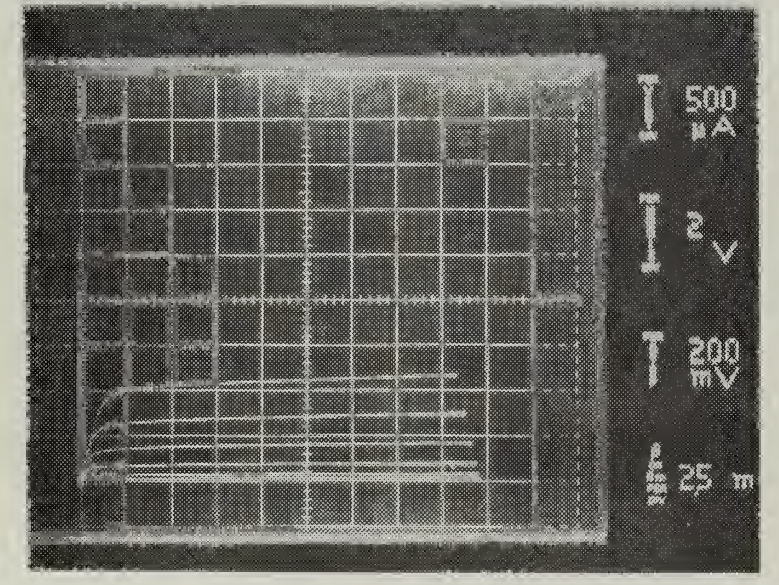
[illegible]

[illegible]

[illegible]

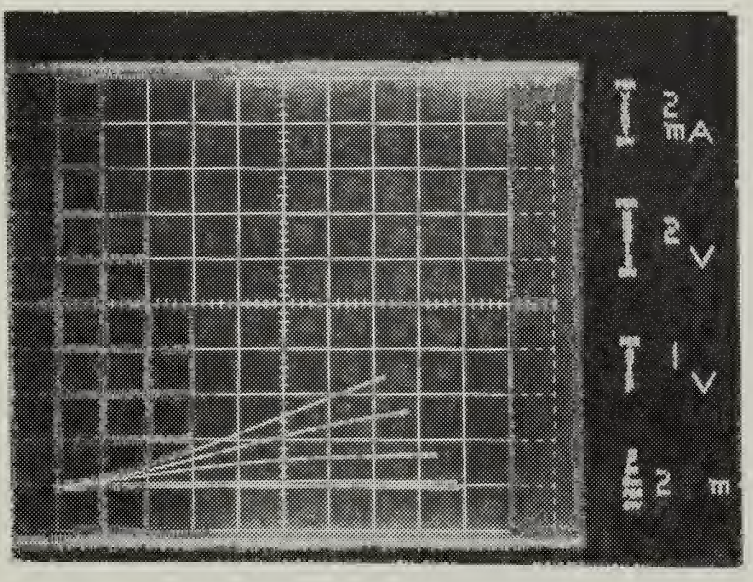


a) Positive Gate Voltage
(bottom most curve: V_G = 0.V)



b) Negative Gate Voltage
(topmost curve: V_G = 0.V)

Figure 9-4. MOSFET I_{dS}-V_{dS} Characteristics after a Total Accumulated Dosage of $6.3X10^{13}$ e/cm^2



Positive Gate Voltage

Figure 9-5. MOSFET I_{dS}-V_{dS} Characteristics after a Total Accumulated Dosage of 2.063X10^{15} e/cm^{2}

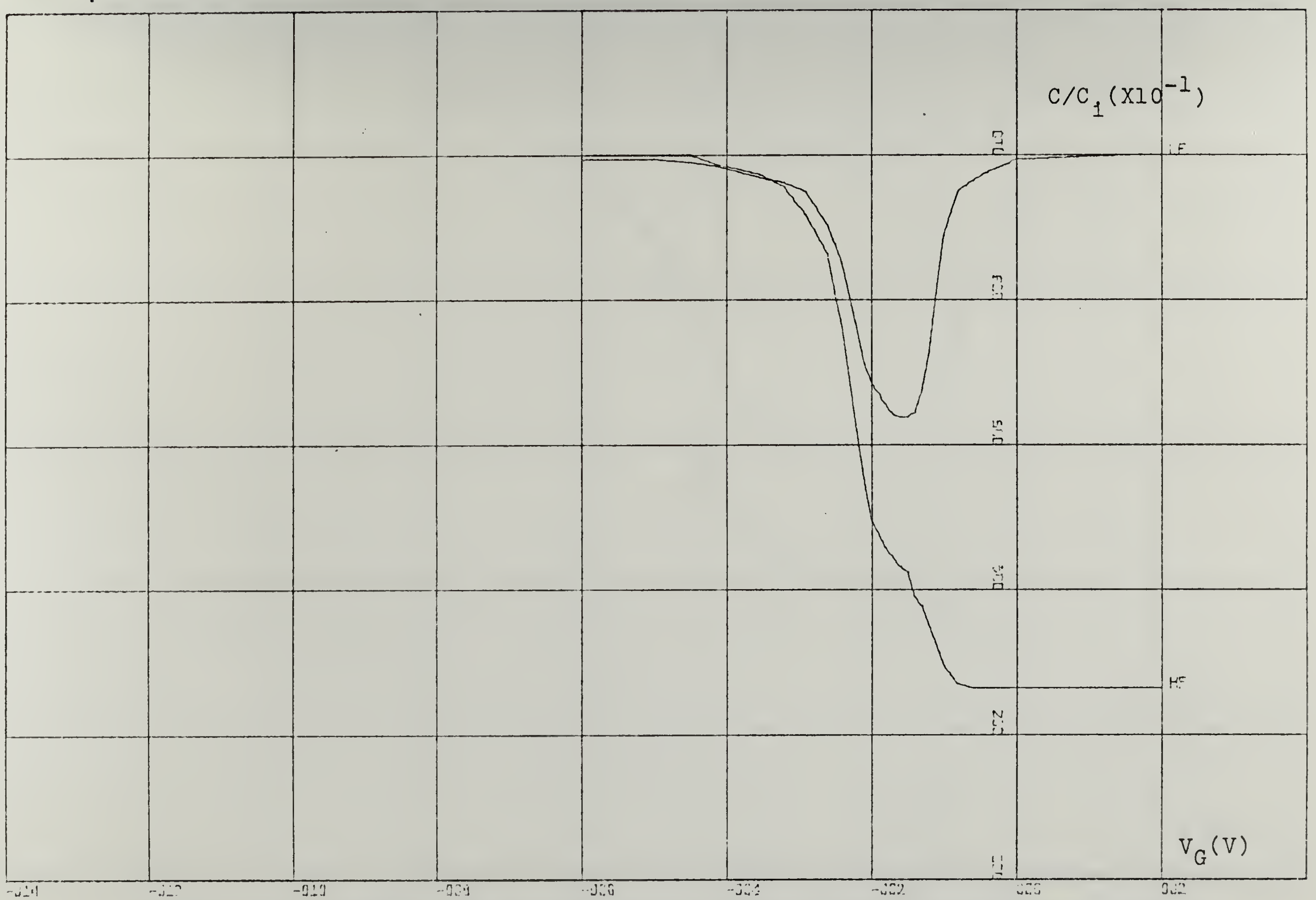


Figure 9-6. MOSFET C-V Characteristics after a Total Accumulated Dosage of $3X10^{12}$ e/cm^2

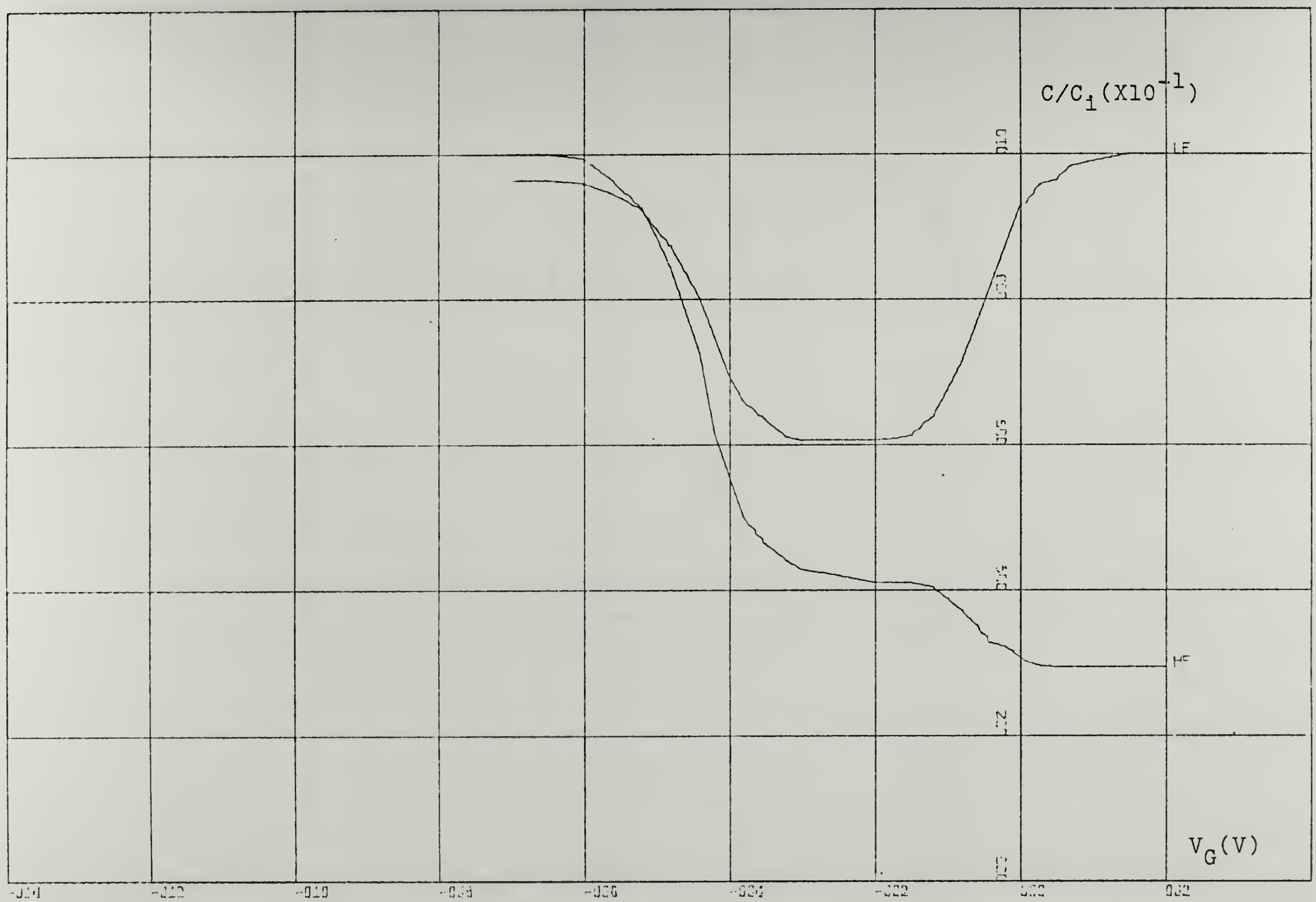


Figure 9-7. MOSFET C-V Characteristics after a Total Accumulated Dosage of $6.3X10^{13}$ e/cm^2

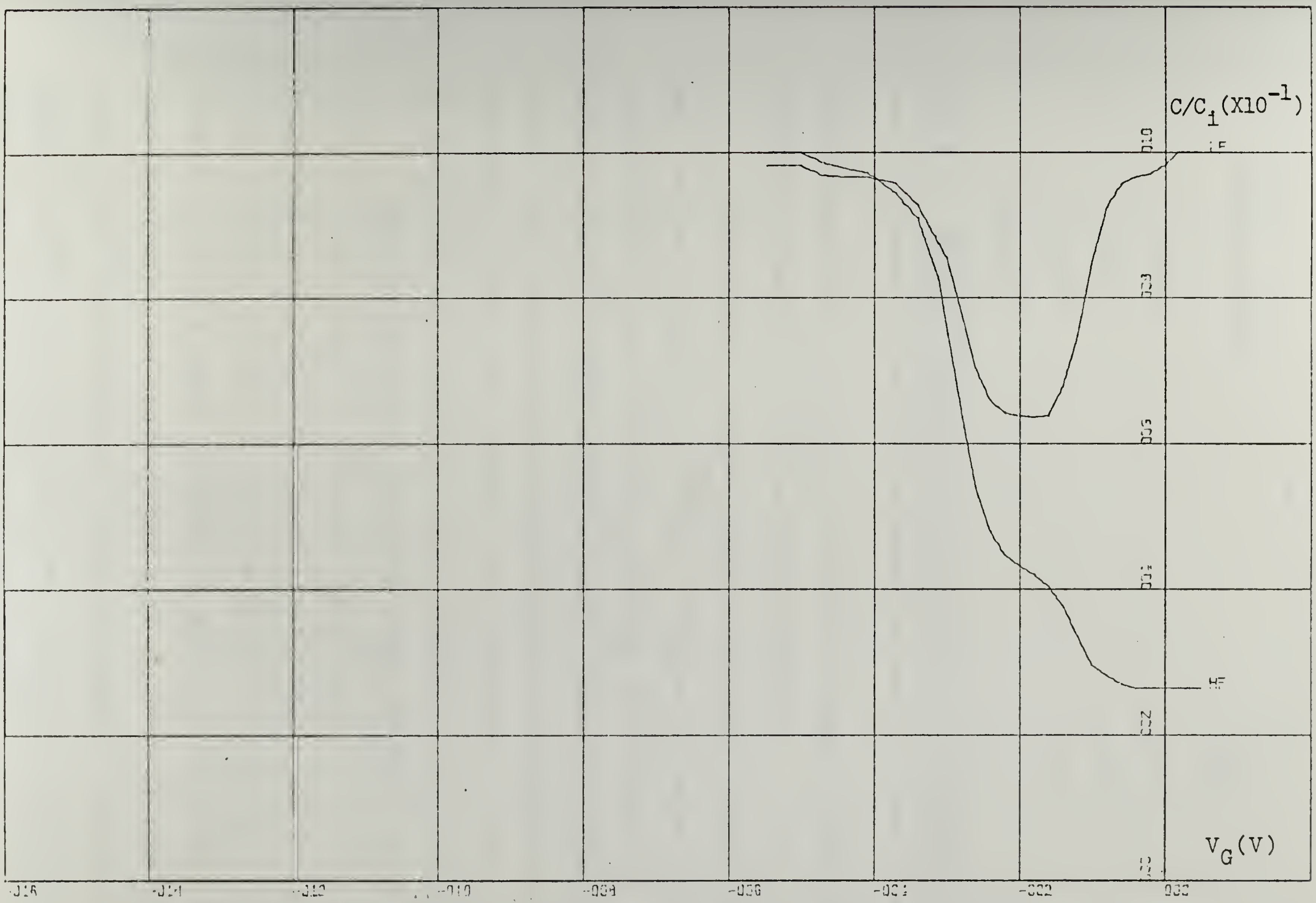


Figure 9-8. MOSFET C-V Characteristics after a Total Accumulated Dosage of 2.063×10^{15} e/cm^2

Dosage (e/cm^2)	V_{th}
0	-1.45
$1X10^{12}$	-1.30
$2X10^{12}$	-1.20
$6.3X10^{13}$	-0.80
$2.063X10^{15}$	$>$ 0

Table X. MOSFET Threshold Voltage Shift as a Function of Total Accumulated Dosage

state density and 3) Q_{eff}-V_S, effective charge in the insulator as a function of the surface potential.

The relation between surface potential and applied gate voltage changed considerably. Figure 9-9 shows this relationship before irradiation and Fig. 9-10 shows the effect after the third radiation step. These two figures reveal that the flatband voltage becomes more negative and the entire curve shifts upward with irradiation. This change is caused by the ionization traps created in the insulator.

The change in the interface state density versus ψ curve is represented in Fig. 9-11 before and 9-12 after the third radiation step. The trend after steps 1 and 2 was to shift the peak of the curve to the left. In Fig. 9-12, however, the peak which occurred at about -0.8V in Fig. 9-11 has disappeared and another peak with an order of magnitude less at 2.5V has appeared. The disappearance of the first peak is unexplained. This peak was expected to continue to move to the left on increased irradiation.

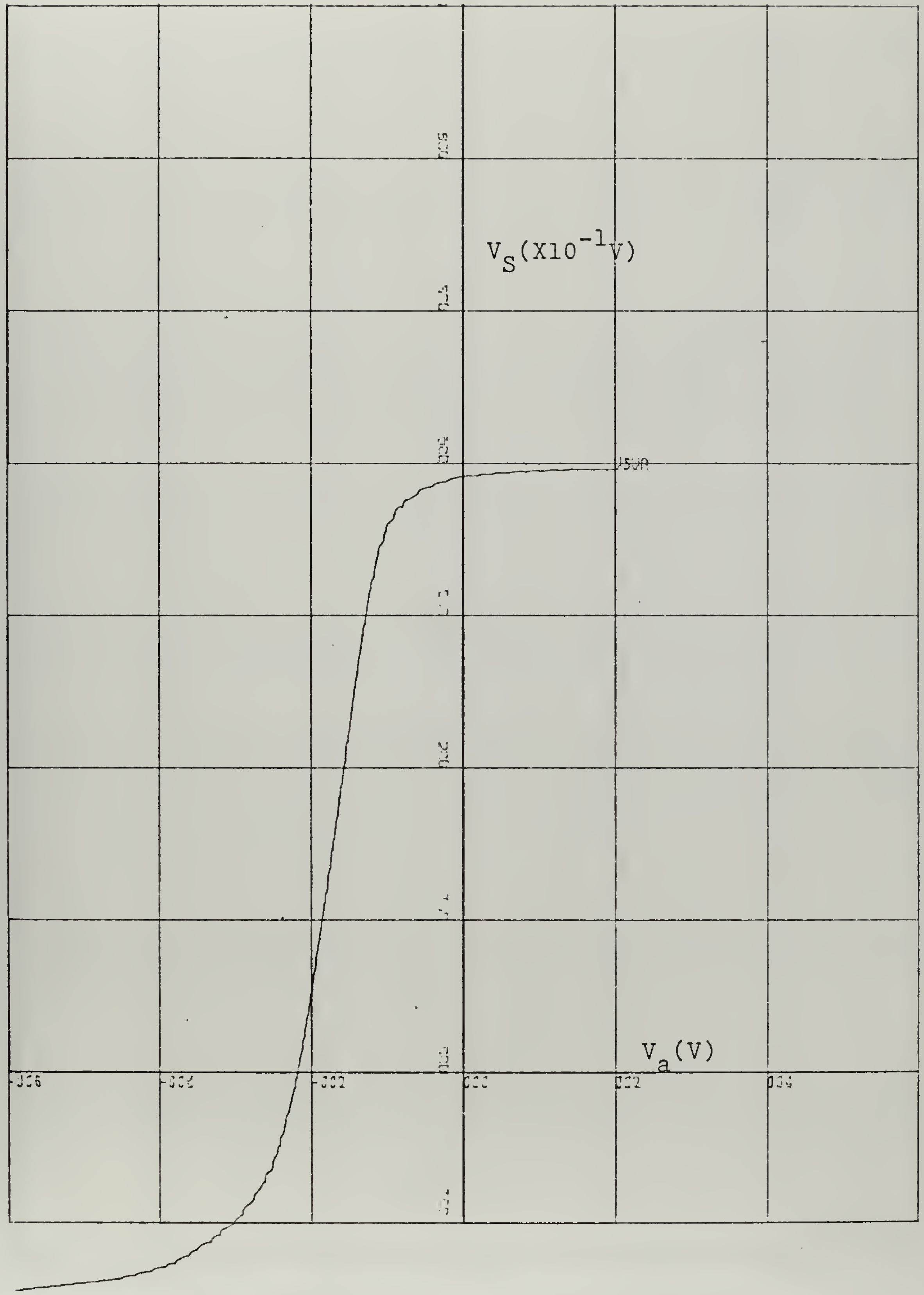


Figure 9-9. MOSFET V_S-V_a Characteristics after a Total Accumulated Dosage of $3X10^{12}$ e/cm^2

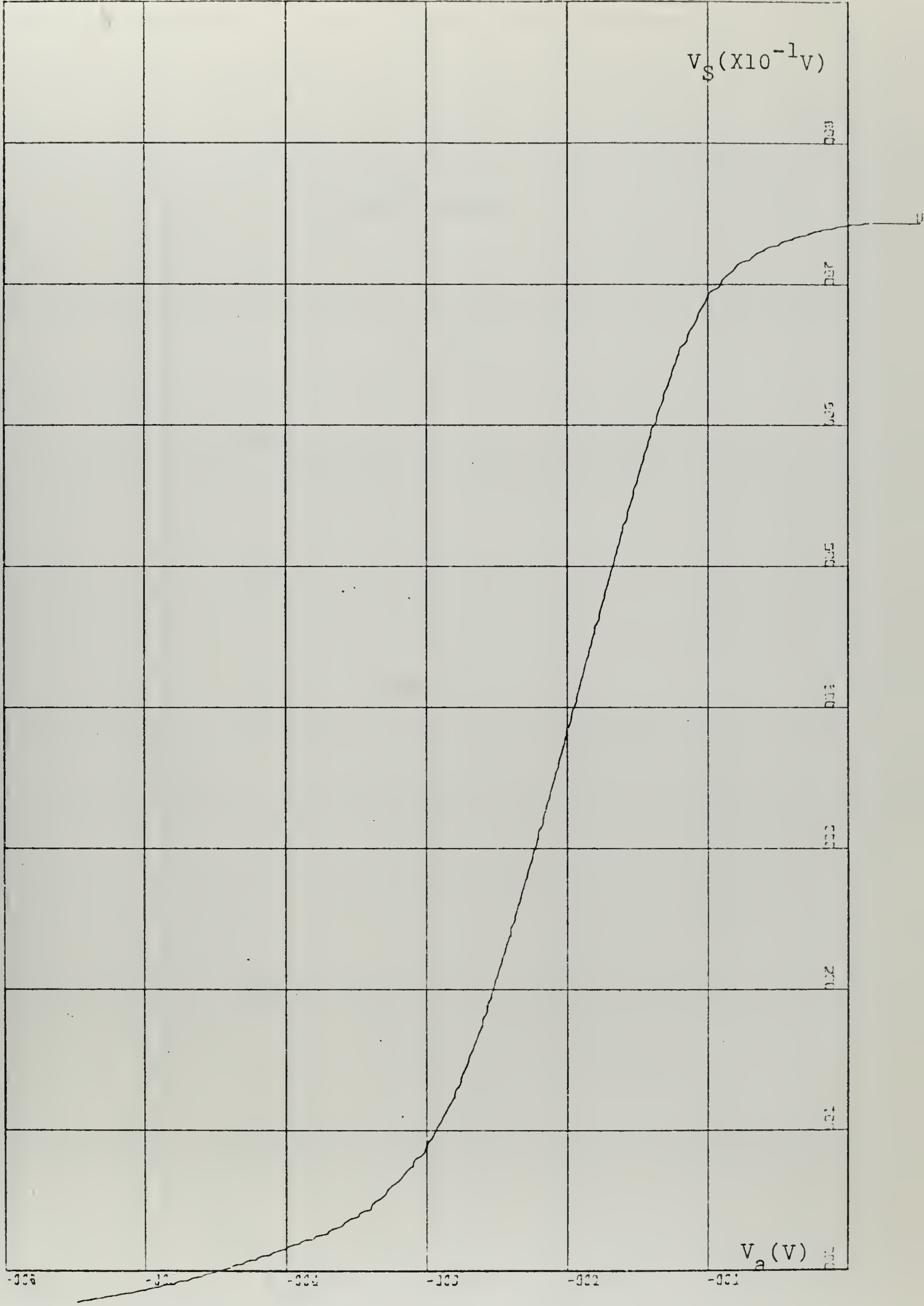


Figure 9-10. MOSFET V_S-V_a Characteristics after a Total Accumulated Dosage of $6.3X10^{13}$ e/cm^2

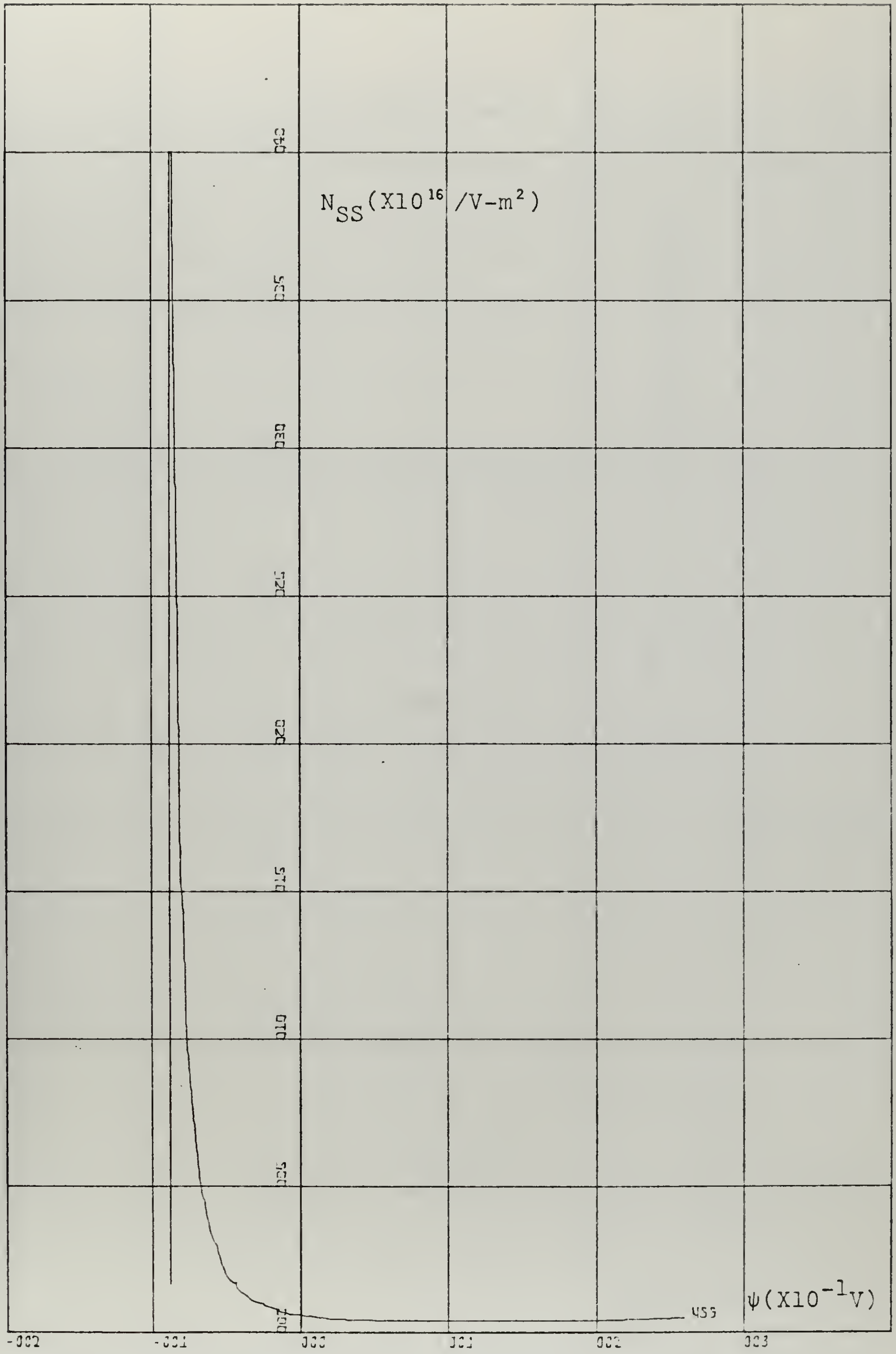


Figure 9-11. MOSFET N_{SS} - V_S Characteristics after a Total Accumulated Dosage of 3X10^{13} e/cm^2

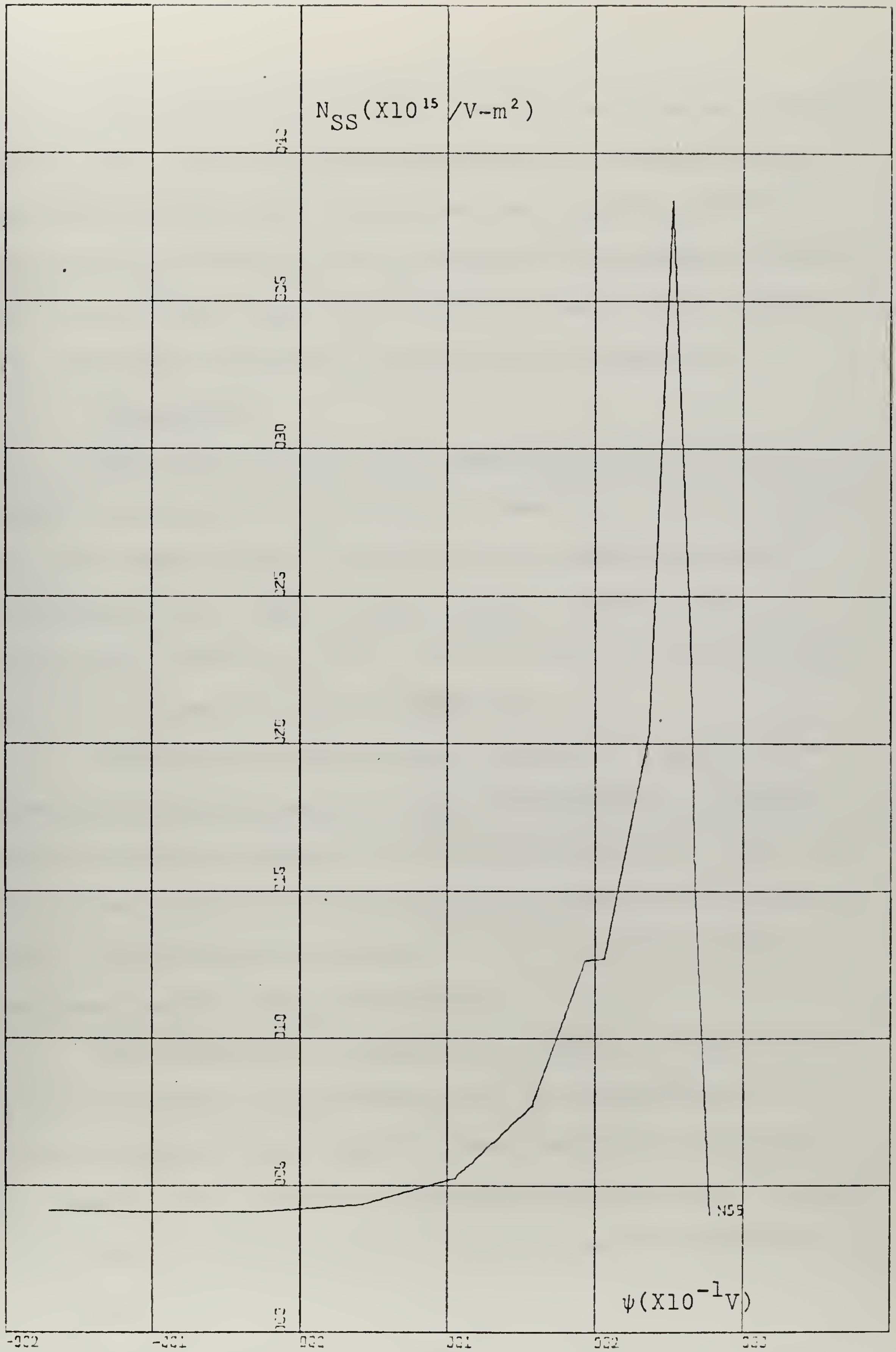


Figure 9-12. MOSFET N_{SS} - V_S Characteristics after a Total Accumulated Dosage of $6.3X10^{13}$ e/cm^2

The effective insulator charge also changes considerably after the third bombardment step. Initially Q_{eff} was approximately $1X10^{-3}$coul/m^2 at zero surface potential and decreased gradually to 0.35V where it decreased sharply. After bombardment Q_{eff} was $2.5X10^{-3}$ at zero surface potential decreased rapidly to 0.10V where it leveled off.

4. Discussion

The effect of electron bombardment shows that the MOSFET is vulnerable to radiation damage to such an extent that it changed from a depletion to an enhancement MOSFET of poor quality. This drastic change occurred after an accumulated dosage of $2X10^{15}$ e/cm^2 which was received after an e-beam exposure time of 10 minutes.

The electron bombardment closed the channel since more positive threshold voltages were required to support drain-to-source current as the dosage increased. This fact is apparent since the drain-to-source current for a particular drain-to-source voltage at various gate voltages decreased as the dosage increased.

The bombardment widened the valley in the low-frequency C-V curve and stretched out the accumulation to inversion region on the high-frequency curve.[35] The effect is caused by the creation of interface states and on ionization traps in the insulator. With increased dosages the

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[35] Similar effects were produced by gamma radiation of 0.5 to 0.7 megarads exposure to MOS capacitors [28].

surface potential versus applied voltage shifted upward and the corresponding flatband voltage became more negative. Both the surface state density and effective insulator charge were affected considerably by the irradiation.

X. CONCLUSION

Three MIS studies were made.

(1) MIS of IV-VI compounds and alloy semiconductors:

The purpose was to develop a fabrication procedure for MIS of PbTe, PbSe, PbSnTe and PbSnSe and to investigate whether their interface qualities are adequate for infrared CCI applications.

To fabricate MIS samples, 3 to 10μ thick thin-films of these semiconductors were first deposited on CaF_2 or BaF_2 substrates followed by e-gun deposition of 100-450A° thick Al_2O_3 or SiO_2 insulating layers. Hg probes were used as metal gates.

The C-V and C-t of the MIS samples were measured mostly at 300°K and on selected samples at 77°K. It was found that both Al_2O_3 and SiO_2 layers showed considerable leakage. Capacitance measurements were distorted. In spite of this difficulty, C-V variations have been obtained which indicated that accumulation, depletion and inversion behaviors occurred and MIS of these IV-VI compounds and alloy semiconductors behave qualitatively like that of Si-MOS.

However, quantitative comparisons of the measured C-V results with theoretical calculations revealed that the following discrepencies exist:

a. The measured change of MIS capacitance from accumulation to inversion is up to 5 times larger than calculated values in some cases.

b. The measured voltage bias range of the transition from accumulation to inversion is up to 4 times larger than the calculated values.

c. Some unexpected temperature variations of the MIS capacitance were found. It was found that the accumulation capacitance varied with the temperature.

It should be noted that similar problems existed in the early stage of the development of Si-MOS. These discrepancies suggested that the following improvements of this research should be made:

a. A deposition procedure of good insulator must first be developed. Insulators other that Al_2O_3 and SiO_2 having large dielectric constants should be used. It is believed that the leakage is the major cause of much of the difficulty.

b. If good insulation materials can not be developed for use with these semiconductors, then the possible use of a double junction MIS should be investigated.

c. After the successful development of good insulator or double junction MIS, the surface preparation of the semiconductor and post treatment of MIS such as annealing can then be pursued to improve the quality of MIS for possible IRCCI applications.

d. Low-frequency measurement and low-temperature measurement must be improved in order that the computer program developed in this thesis can be successfully used to analyze the basic physical parameters of these MIS which are necessary to build up a good understanding of their behaviors.

(2) MIS of Ge:

Both n and p-type Ge-MIS have been made by e-gun deposition of 180 to 250A° of Al_2O_3. Their resistivity are 40Ω -cm and 0.05Ω -cm respectively. C-V and C-t measurements indicated that they behave qualitatively like Si-MOS. Analysis of these data showed that the interface state densities and the flatband voltages are:

Quantity	0.05Ω -cm (p)	40.0Ω -cm (n)
$N_{SS}(V^{-1}m^{-2})$	$4X10^{16}$	$2.5X10^{17}$
V_{fb} (V)	-1.20	———

The Ge-MIS C-V characteristics were not similar at all gate locations. It is suggested that sample fabrication techniques be improved to eliminate these nonuniformities.

(3) Effect of electron bombardment on n-channel Si depletion MOSFET:

65.4Mev electron bombardments were carried out in the Naval Postgraduate School Linear Electron Accelerator. Doses of 10^{12} , $6X10^{13}$, and $2X10^{15}$ were used. It was found that the most sensitive change is the decrease of threshold voltage. Before bombardment, the V_{th} was -1.45V after a dose of $2X10^{15}$ e/cm^2 , V_{th} became positive, which changed the MOSFET from depletion to enhancement.

```
NA-ND = 0.130E 18
OXIDE THICKNESS(MICRONS) = 0.0250
FLATBAND CAPACITANCE =  0.77416
CO =0.3117E-06
CINT =0.2200E 14
TEMP =    300.000
EG(EV) =       0.803
                                                                DEPL. LAYER        SURFACE                            Q STORAGE
   GATE VOLTAGE      LOW FREQ. CAP.      HIGH FREQ. CAP.     WIDTH(METERS)      POTENTIAL        DEPL. CAP.        (1/SQ.CM.)

      -9.00            0.99415                                                   -0.220
      -4.32            0.98773                                                   -0.181
      -2.08            0.97454                                                   -0.142
      -0.99            0.94858                                                   -0.103
      -0.43            0.90195                                                   -0.065
      -0.13            0.83092                                                   -0.026
       0.05            0.74503                                                    0.013
       0.19            0.66296                                                    0.052
       0.29            0.59642                                                    0.090
       0.38            0.54603                                                    0.129
       0.46            0.50785                                                    0.168
       0.54            0.47805                                                    0.207
       0.57            0.46650            0.46650            0.5198E-07           0.224          0.45814          0.92973E 10
       0.64            0.44456            0.44439            0.5683E-07           0.263          0.43715          0.90579E 10
       0.71            0.42659            0.42581            0.6129E-07           0.302          0.41942          0.88485E 10
       0.78            0.41334            0.40983            0.6545E-07           0.341          0.40408          0.87142E 10
       0.84            0.41116            0.39589            0.6936E-07           0.380          0.39051          0.88373E 10
       0.97            0.53773            0.37490            0.7579E-07           0.449 T        0.36778          0.13441E 11
       1.04            0.66788            0.36829            0.7797E-07           0.475          0.35755          0.21656E 11
       1.14            0.80026            0.36247            0.7995E-07           0.501          0.34336          0.42262E 11
       1.31            0.89055            0.35769            0.8162E-07           0.527          0.32196          0.91295E 11
       1.64            0.93963            0.35410            0.8291E-07           0.552          0.29139          0.19976E 12
       2.21            0.96527            0.35165            0.8381E-07           0.578          0.25356          0.42192E 12
       3.19            0.97939            0.35008            0.8438E-07           0.604          0.21321          0.84935E 12
       4.82            0.98758            0.34911            0.8475E-07           0.630          0.17474          0.16364E 13
       7.53            0.99247            0.34852            0.8497E-07           0.656          0.14067          0.30430E 13
      11.98            0.99543            0.34816            0.8510E-07           0.682          0.11191          0.55060E 13
      19.32            0.99723            0.34794            0.8518E-07           0.707          0.08834          0.97557E 13

 SURFACE POTENTIAL    DEPLETION DEPTH     INSULATOR           SEMICONDUCTOR
  (DEEP DEPLETION)    (DEEP DEPLETION)    FIELD STRENGTH      FIELD STRENGTH
      (VOLTS)         (CENTIMETERS)         (VOLTS/CM)          (VOLTS/CM)

   0.5712775E 00      0.8815950E-05        0.2357E 03           0.6480E 05
   0.6424191E 00      0.9348777E-05        0.2499E 03           0.6872E 05
   0.7110498E 00      0.9835481E-05        0.2629E 03           0.7229E 05
   0.7778112E 00      0.1028686E-04        0.2750E 03           0.7561E 05
   0.8435824E 00      0.1071296E-04        0.2864E 03           0.7874E 05
   0.9704495E 00      0.1149032E-04        0.3071E-01           0.8446E 05
   0.1035656E 01      0.1187007E-04        0.3174E-01           0.8725E 05
   0.1135823E 01      0.1243085E-04        0.3326E-01           0.9137E 05
   0.1312745E 01      0.1336398E-04        0.3574E-01           0.9823E 05
   0.1636371E 01      0.1492060E-04        0.3990E-01           0.1097E 06
   0.2209889E 01      0.1733926E-04        0.4639E-01           0.1275E 06
   0.3188493E 01      0.2082756E-04        0.5569E-01           0.1531E 06
   0.4821992E 01      0.2561290E-04        0.6847E-01           0.1883E 06
   0.7523407E 01      0.3199285E-04        0.8553E-01           0.2352E 06
   0.1197690E 02      0.4036620E-04        0.1079E 00           0.2967E 06
   0.1931329E 02      0.5125943E-04        0.1373E 00           0.3768E 06
GRAPH TITLED
    GERMANIUM  NA=1.3E17   T=300   X=250A
    KOST             P-TYPE SUBSTRATE
HAS BEEN PLOTTED.
```

```
      PROGRAM TO COMPUTE THE SURFACE POTENTIAL,IMPURITY
      CONCENTRATION,INTERFACE STATE DENSITY,AND EFFECTIVE
      SURFACE CHARGE IM MIS STRUCTURES FROM READ IN
      EXPERIMENTAL CAPACITANCE VS VOLTAGE HIGH AND LOW
      FREQUENCY CURVES




C     THE PARAMETERS USED INCLUDE(ALL MKS UNITS):
C     AREA=AREA OF GATE
C     BOLTZ=BOLTZMANN'S CONSTANT
C     EPO=PERMITTIVITY OF FREE SPACE
C     Q=ELECTRONIC CHARGE
C     ENI=INTRINSIC CARRIER CONSENTRATION
C     T=TEMPERATURE
C     ERS=DIELECTRIC CONSTANT OF SEMICONDUCTOR
C     ERO=DIELECTRIC CONSTANT OF INSULATOR
C     XO=INSULATOR THICKNESS
C     COL=LOW FREQUENCY ACCUMULATION CAPACITANCE
C     CLONEW=LOW FREQUENCY CORRECTED COL FOR AL2O3
C     COH=HIGH FREQUENCY ACCUMULATION CAPACITANCE
C     CLO=LOW FREQUENCY CAPACITANCE
C     VA=LOW FREQUENCY GATE VOLTAGE
C     CHI=HIGH FREQUENCY CAPACITANCE
C     VH=HIGH FREQUENCY GATE VOLTAGE
C     VS=POTENTIAL AT INTERFACE SURFACE OF SEMICONDUCTOR
C     ENS=IMPURITY CONCENTRATION AT SEMICONDUCTOR SURFACE
C     ENB=IMPURITY CONCENTRATION IN SEMICONDUCTOR BULK
C     PF=PICOFARAD
C     PHIB=POTENTIAL IN SEMICONDUCTOR BULK
C     NSS=INTERFACE STATE DENSITY
C     QEFF=EFFECTIVE INTERSTATE CHARGE


      DIMENSION VS(500),VA(500),CH(500),VH(500),ID(19),
     1CL(500),CLO(500),CHI(500)
      DATA IDN/4HIDN /,IDP/4HIDP /
      N=0
    1 READ(5,9,END=100) NAME,AREA,CLONEW
    9 FORMAT(A4,6X,E10.3,F10.3)
      IF(AREA.EQ.0.) GO TO 1
      READ(5,10) BOLTZ,EPO,Q,ENI
   10 FORMAT(4E15.5)
      READ(5,11) T,ERS
   11 FORMAT(2F10.3)
      VTH=(BOLTZ*T)/Q
      EPS=ERS*EPO
      READ(5,20) COL
   20 FORMAT(F10.3)
      DO 30 I=1,500
      READ(5,25) VA(I),CLO(I)
   25 FORMAT(2F10.3)
      IF(VA(I).EQ.500.0) GO TO 31
      CL(I)=CLO(I)/COL
   30 CONTINUE
   31 NL = I-1
      READ(5,40) COH
   40 FORMAT(F10.3)
      DO 50 I=1,500
      READ(5,45) VH(I),CHI(I)
   45 FORMAT(2F10.3)
      IF(VH(I).EQ.500.0) GO TO 51
      CH(I)=CHI(I)/COH
   50 CONTINUE
   51 NH = I-1
      IF (AREA.GT.1.0E-10) GO TO 53
      READ(5,52) ERO,XO,PF
   52 FORMAT(F10.3,2E15.3)
      AREA=(COH*PF*XO)/(ERO*EPO)
      WRITE(6,54) AREA
```

```
   54 FORMAT(6X,E9.3)
   53 IF(NL.EQ.0.OR.NH.EQ.0.OR.NL.GT.500.OR.NH.GT.500) GO
     1TO 1
      N=N+1
      IF(CLONEW.NE.0.) COL = CLONEW
      READ(5,60) WHAT
   60 FORMAT(F10.1)
C     WHAT INDICATES TYPE OF PLOT DESIRED
C     IF(WHAT.LT.0) POINT PLOT
C     IF(WHAT.EQ.0) POINT AND SMOOTH CURVE PLOT
C     IF(WHAT.GT.0) SMOOTH CURVE PLOT
      CALL VSOFVA(VS,ENS,ENB,COL,CL,VA,NL,COH,CH,VH,NH,AREA
     1,EPS,VTH,ENI,WHAT)
      IF(NAME.EQ.IDN.OR.NAME.EQ.IDP) GO TO 1
      CALL STATES(ENB,VS,CL,CH,VA,NL,AREA,EPS,VTH,ENI,WHAT)
      CALL QEFF(ENS,ENB,VS,VA,NL,CH,COL,AREA,EPS,VTH,ENI
     1,WHAT)
      GO TO 1
      END
  100 CONTINUE

C     SUBROUTINE VSOFVA PROVIDES PLOTS OF:
C     (C/CS)**2 - US   CLF - VL   CHF - VL   VS - VA
C     AND PROVIDES TABULAR DATA ON: ENS ENB PHIB


      SUBROUTINE VSOFVA(VS,ENS,ENB,COLO,CLN,VL,NL,COHI,CHN,
     1VH,NH,AREA,EPS,VTH,ENI,WHAT)
      DIMENSION VS(500),CLN(500),VL(500),CHN(500),VH(500),
     1F(500),G(500),H(500),X(500),RANGE(4)
      DATA PI/3.14159/,Q/1.602E-19/,RUP/0.75/,RLO/0.95/,
     1PF/1.0E-12/
      REAL*8 TITL1(12),TITL2(12),TITL3(12)
      REAL LABL1/'C-US'/,LABL2/'SFIT'/,LABL3/' LF '/
      REAL LABL4/' HF '/,LABL5/'DEPL'/,LABL6/'REGN'/
      REAL LABL7/'VSVA'/
      READ(5,101) TITL1,TITL2,TITL3
  101 FORMAT(6A8)
       CHNMIN=SMALL(CHN,NH)
       CUPPER=1.-RUP*(1.-CHNMIN)
       CLOWER=1.-RLO*(1.-CHNMIN)
       NUS=0
       CSMIN=CHNMIN*COHI/(1.-CHNMIN)
       DO 1 I=1,NL
       F(I)=1.-CLN(I)
       IF(F(I).LT.0.) F(I) = 0.
    1 CONTINUE
C      WE NOW HAVE 1.-C/CO(LF) IN
       CALL SUMUP(F,VL,VS,NL)
       DO 2 I=1,NL
       F(I)=FTP(VL(I),CHN,VH,NH)
       G(I)=(1./F(I)-1.)**2
       IF(F(I).GT.CUPPER.OR.F(I).LT.CLOWER) GO TO 2
       NUS=NUS+1
       H(NUS)=G(I)
       X(NUS)=VS(I)
    2 CONTINUE
C      F NOW CONTAINS C/CO(HF) WRT VL
C      G NOW CONTAINS (CO/CS)**2 WITH RESPECT TO VL OR VS
C      H AND X CONTAIN POINTS FROM G AND VS FOR STLFIT
       VA = FTP(X(1),VL,VS,NL)
       VB = FTP(X(NUS),VL,VS,NL)
       CALL STLFIT(H,X,NUS,SLOPE,YCEPT)
       USO=-YCEPT/SLOPE
       H(2)=1.1*BIGST(G,NL)
       X(2)=(H(2)-YCEPT)/SLOPE
       H(1)=-.2*H(2)
       X(1)=(H(1)-YCEPT)/SLOPE
       IF(X(1).LT.X(2)) GO TO 5
       XTR = X(1)
       X(1) = X(2)
       X(2) = XTR
```

```
          XTR = H(1)
          H(1)  = H(2)
          H(2)  = XTR
C         H AND X CONTAIN NOW THE STLFIT STRAIGHT LINE
        5 WRITE(6,12)
       12 FORMAT('1',' (CO/CS)**2 - US  PLOT ')
          RANGE(1)=0.8
          RANGE(2)=-0.10
          RANGE(3)=2.0
          RANGE(4)=-0.1
          IF (WHAT) 50,51,52
       50 CALL UTPLOT(VS,G,NL,RANGE,1,1)
          CALL UTPLOT(X,H,2,RANGE,1,3)
          GO TO 53
       51 CALL UTPLOT(VS,G,NL,RANGE,1,1)
          CALL UTPLOT(X,H,2,RANGE,1,3)
       52 CALL DRAW(NL,VS,G,1,0,LABL1,TITL1,0.0,0.0,0,0,0,0,
         16,9,1,LAST)
          CALL DRAW(2,X,H,3,0,LABL2,TITL1,0.0,0.0,0,0,0,0,6,9,
         1LAST)
       53 CONTINUE
          DO 3 I=1,NL
          CLN(I) = COLO*CLN(I)
        3 CHN(I) = COHI*F(I)
C         CLN AND CHN NOW CONTAIN C(LF) AND C(HF) WRT VL
          WRITE(6,13)
       13 FORMAT('1','  CLN & CHN - VL  PLOT ')
           F(1) = FTP(VA,CHN,VL,NL)
           F(2) = .75*CHNMIN*COHI
           G(1) = VA
           G(2) = VA+1.E-3
           H(1) = FTP(VB,CHN,VL,NL)
           H(2) = F(2)
           X(1) = VB
           X(2) = VB+1.E-3
C         F,G,H,ANDX NOW CONTAIN DEPL. REGION MARKERS
          RANGE(1)=4.0
          RANGE(2)=-8.0
          RANGE(3)=COLO+1.0
          RANGE(4)=.65*CHNMIN*COHI
          IF (WHAT) 60,61,62
       60 CALL UTPLOT(VL,CLN,NL,RANGE,1,1)
          CALL UTPLOT(VL,CHN,NL,RANGE,1,2)
          CALL UTPLOT(G,F,2,RANGE,1,2)
          CALL UTPLOT(X,H,2,RANGE,1,3)
          GO TO 63
       61 CALL UTPLOT(VL,CLN,NL,RANGE,1,1)
          CALL UTPLOT(VL,CHN,NL,RANGE,1,2)
          CALL UTPLOT(G,F,2,RANGE,1,2)
          CALL UTPLOT(X,H,2,RANGE,1,3)
       62 CALL DRAW(NL,VL,CLN,1,0,LABL3,TITL2,4.0,0.0,0,0,0,0,
         16,9,1,LAST)
          CALL DRAW(NL,VL,CHN,2,0,LABL4,TITL2,4.0,0.0,0,0,0,0,
         16,9,1,LAST)
          CALL DRAW(2,G,F,2,0,LABL5,TITL2,4.0,0.0,0,0,0,0,
         16,9,1,LAST)
          CALL DRAW(2,X,H,3,0,LABL6,TITL2,4.0,0.0,0,0,0,0,
         16,9,1,LAST)
       63 CONTINUE
           ENS=-2.*COHI**2/(EPS*Q*AREA**2*SLOPE)*PF**2
           ENB = SIGN(QEY(CSMIN*PF,AREA,VTH,EPS,ENI),ENS)
           PHIB  = SIGN(VTH*ALOG(ABS(ENB)/ENI),ENS)
          WRITE(6,89)
       89 FORMAT('1','  VS - VA  ')
          WRITE(6,90) ENS,ENB,PHIB
       90 FORMAT(//,' IMPURITY CONCENTRATION',//8X,'ENS = ',
         11PE9.2,' PER CUBIC METER',/8X,'ENB = ',E9.2,
         2' PER CUBIC METER',/8X,'PHIB = ',0PF6.3,' VOLTS')
          VSO=-VTH*ABS(ENB)/ENS-(ENS-ENB)/ENS*PHIB/2.
          DELTA=VSO-USO
          DO 4 I=1,NL
        4 VS(I)=VS(I)+DELTA
```

```
      RANGE(1)=4.0
      RANGE(2)=-8.0
      RANGE(3)=1.0
      RANGE(4)=-0.5
      IF (WHAT) 70,71,72
   70 CALL JTPLOT(VL,VS,NL,RANGE,1,0)
      GO TO 73
   71 CALL UTPLOT(VL,VS,NL,RANGE,1,0)
   72 CALL DRAW(NL,VL,VS,0,0,LABL7,TITL3,0.0,0.0,0,0,0,0,
     16,9,1,LAST)
   73 CONTINUE
  100 RETURN
      END
C
C     SUBROUTINE STATES PROVIDES A PLOT OF NSS-PSI AND
C     TABULAR DATA ON NSS AT THREE VALUES OF PSI


      SUBROUTINE STATES(ENB,VS,CLF,CHF,VA,NLF,AREA,EPS,VTH,
     1ENI,WHAT)
      DIMENSION VS(500),CLF(500),CHF(500),VA(500),PSI(500),
     1ENSS(500),RANGE(4)
      DATA PI/3.14159/,PF/1.0E-12/,Q/1.602E-19/
      REAL*8 TITL4(12)
      REAL LABL8/' NSS'/
      READ(5,104) TITL4
  104 FORMAT(6A8)
       COL=BIGST(CLF,NLF)
       COH=BIGST(CHF,NLF)
       NSS=0
       F=PF/(AREA*Q)
       PHIB=VTH*ALOG(ABS(ENB)/ENI)
       IF(ENB.LT.0.)PHIB=-PHIB
       U1=AMIN1(-1.7*PHIB,0.)
       U2=AMAX1(-1.7*PHIB,0.)
       DO 10 I=1,NLF
       IF(VS(I).LT.U1.OR.VS(I).GT.U2)GO TO 10
       NSS=NSS+1
       PSI(NSS)=-(PHIB+VS(I))
       ENSS(NSS)=(COL*CLF(I)/(COL-CLF(I))-COH*CHF(I)/
     1(COH-CHF(I)))*F
       IF(ENSS(NSS).LT.0.)ENSS(NSS)=0.
   10 CONTINUE
      IF(NSS.GT.2) GO TO 5
      WRITE(6,90)
   90 FORMAT(///' VS DATA INADEQUATE FOR NSS CALCULATION')
      GO TO 100
    5 LAST = NSS/2
       DO 11 I=1,LAST
       J = NSS-I+1
       X = PSI(J)
       PSI(J) = PSI(I)
       PSI(I) = X
       X = ENSS(J)
       ENSS(J) = ENSS(I)
   11 ENSS(I) = X
      X=FTP(0.,ENSS,PSI,NSS)
      Y=0.
      WRITE(6,8)
    8 FORMAT('1','  NSS - PSI PLOT')
      WRITE(6,9)ENSS(1),PSI(1),X,Y,ENSS(NSS),PSI(NSS)
    9 FORMAT(//,' INTERFACE STATE DENSITY'//9X,3HNSS,10X,
     13HPSI/6X,'( /VM**2 )     ( VOLTS )'//3(6X,1PE9.2,
     22X,0PF8.3/))
      RANGE(1)=0.3
      RANGE(2)=-0.2
      RANGE(3)=4.0E17
      RANGE(4)=4.0E15
       IF (WHAT) 80,81,82
   80 CALL UTPLOT(PSI,ENSS,NSS,RANGE,1,0)
      GO TO 83
   81 CALL UTPLOT(PSI,ENSS,NSS,RANGE,1,0)
```

```
   82 CALL DRAW(NSS,PSI,ENSS,0,0,LABL8,TITL4,0.1,0.0,0,0,0,0
     1,6,9,1,LAST)
   83 CONTINUE
  100 RETURN
       END
C     SUBROUTINE QEFF PROVIDES A PLOT OF QEFF-VS AND TABULAR
C     DATA ON QEFF NEFF AT THREE VALUES OF VS


      SUBROUTINE QEFF(ENS,ENB,VS,VA,NLF,CHF,COL,AREA,EPS,
     1VTH,ENI,WHAT)
      DIMENSION VS(500),VA(500),CHF(500),QFF(500),VF(500),
     1RANGE(4)
      DATA Q/1.602E-19/,PI/3.14159/,PF/1.0E-12/
      INTEGER QEFF/4HQEFF/,LOGQ/4HLOGQ/
      REAL*8 TITL5(12)
      REAL LABL9/'QEFF'/
      READ(5,105) TITL5
  105 FORMAT(6A8)
       COH=BIGST(CHF,NLF)
       F=Q*EPS*AREA**2
       R=2.*(ENI/ENB)**2
       NFF=0
       PHIB=SIGN(VTH*ALOG(ABS(ENB)/ENI),ENB)
       U1=AMIN1(0.,-1.7*PHIB)
       U2=AMAX1(0.,-1.7*PHIB)
       DO 10 I=1,NLF
       IF(VS(I).LT.U1.OR.VS(I).GT.U2) GO TO 10
       NFF=NFF+1
       VF(NFF)=VS(I)
       X=VF(NFF)/VTH
       IF(ENB.LT.0.)X=-X
       QFF(NFF)=(COL*(VS(I)-VA(I))*PF-F*(COH-CHF(I))/(COH*
     1CHF(I)*PF)*(ENS-ENB*(EXP(X)+R*SINH(X))))/AREA
   10 CONTINUE
      IF(NFF.GT.2) GO TO 5
      WRITE(6,90)
   90 FORMAT(///' VS DATA INADEQUATE FOR QEFF CALCULATION')
      GO TO 100
    5 Y=-PHIB
       X=FTP(Y,QFF,VF,NFF)
       S1=ABS(QFF(1)/Q)
       S2=ABS(X/Q)
       S3=ABS(QFF(NFF)/Q)
      WRITE(6,8)
    8 FORMAT('1',' QEFF - VS PLOT')
      WRITE(6,9)QFF(1),S1,VF(1),X,S2,Y,QFF(NFF),S3,VF(NFF)
    9 FORMAT(///' EFFECTIVE SURFACE CHARGE, STATE DENSITY'
     1//8X,4HQEFF,8X,4HNEFF,6X,2HVS/5X,'(COUL/M**2)',3X,
     2'(/M**2)',3X,'(VOLTS)'//3(6X,1PE9.2,1X,E11.2,
     31X,0PF8.3/))
      RANGE(1)=0.5
      RANGE(2)=-0.1
      RANGE(3)=1.0E-2
      RANGE(4)=-1.0E-3
      IF (WHAT) 85,86,87
   85 CALL UTPLOT(VF,QFF,NFF,RANGE,1,0)
      GO TO 88
   86 CALL UTPLOT(VF,QFF,NFF,RANGE,1,0)
   87 CALL DRAW(NFF,VF,QFF,0,0,LABL9,TITL5,0.0,0.0,0,0,0,0,
     16,9,1,LAST)
   88 CONTINUE
  100 RETURN
       END
C     SMALL FINDS THE SMALLEST OF X
```

```
      FUNCTION SMALL(X,N)
      DIMENSION X(500)
      SMALL = X(1)
      DO 1 I=2,N
      IF(X(I).LT.SMALL) SMALL = X(I)
    1 CONTINUE
      RETURN
      END
C     SUMUP INTEGRATES BY TRAPEZOIDAL RULE


      SUBROUTINE SUMUP(Y,X,F,NPT)
      DIMENSION Y(500),X(500),F(500)
      F(1) = 0.
      DO 10 I=2,NPT
   10 F(I) = F(I-1) + (X(I)-X(I-1))*(Y(I)+Y(I-1))/2.
      RETURN
      END
C     FTP SETS THE MAXIMUM UPPER AND LOWER LIMITS ON Y


      FUNCTION FTP(VAL,Y,X,NPT)
      DIMENSION X(500),Y(500)
      DATA IC/1/
      IF(IC.GT.NPT) IC=1
      IF(VAL-X(IC)) 1,2,3
    2 FTP = Y(IC)
      GO TO 5
    3 IF(IC.EQ.NPT) GO TO 2
      IC = IC+1
      IF(VAL-X(IC)) 6,2,3
    1 IF(IC.EQ.1) GO TO 2
    6 IC = IC-1
      IF(VAL-X(IC)) 1,2,4
    4 FTP = Y(IC) + (VAL-X(IC))*(Y(IC+1)-Y(IC))/(X(IC+1)-X(I
    5 RETURN
      END
C     STLFIT FITS A STRAIGHT LINE TO A CURVE


      SUBROUTINE STLFIT(Y,X,N,SLOPE,YCEPT)
      DIMENSION Y(500),X(500)
      XBAR = EXPECT(X,N)
      Q = 0.
      A = 0.
      DO 20 I=1,N
      DEV = X(I)-XBAR
      Q = Q+DEV**2
   20 A = A+DEV*Y(I)
      IF(Q.NE.0.) SLOPE = A/Q
      IF(Q.EQ.0.) SLOPE = 0.
      YCEPT = EXPECT(Y,N) - SLOPE*XBAR
      RETURN
      END
C     EXPECT PROVIDES THE SUMMATION OF Z


      FUNCTION EXPECT(Z,N)
      DIMENSION Z(500)
      EXPECT = 0.
      DO 10 I=1,N
      10 EXPECT = EXPECT+Z(I)
      EXPECT = EXPECT/FLOAT(N)
      RETURN
```

```
       END
C     BIGST FINDS THE LARGEST OF X

       FUNCTION BIGST(X,N)
       DIMENSION X(500)
       BIGST = X(1)
       DO 1 I=2,N
       IF(X(I).GT.BIGST) BIGST = X(I)
       1 CONTINUE
       RETURN
       END
C     QEY SOLVES FOR BULK IMPURITY CONCENTRATION

       FUNCTION QEY(CSMIN,AREA,VTH,EPS,ENI)
       DATA PI/3.14159/,Q/1.602E-19/,PF/1.0E-12/
       VAL=VTH*(CSMIN/AREA)**2/(EPS*Q*ENI)
       N=0
       X=13.
       DX=1.
       1 X=X+DX
       IF(EXP(X/2.)/SQRT(2.*(X-2.))-VAL) 1,100,2
       2 DX=+.1*DX
       N=N+1
       IF(N.GT.2) GO TO 100
       3 X=X-DX
       IF(X.LT.3.) GO TO 100
       IF(EXP(X/2.)/SQRT(2.*(X-2.))-VAL) 4,100,3
       4 DX=.1*DX
      GO TO 1
       RETURN
       100 QEY=2.*VTH*(X-2.)*(CSMIN/AREA)**2/(EPS*Q)
       END
```

```
C     PROGRAM TO CALCULATE THE MINIMUM HIGH FREQUENCY
C     CAPACITANCE OF A 4-6 SEMICONDUCTOR, WITH
C     VALUES OF SEMICONDUCTOR DIELECTRIC CONSTANT,
C     VERSUS IMPURITY CONCENTRATION



C   THE INPUTS TO THIS PROGRAM ARE
C     RESC=SEMICONDUCTOR RELATIVE DIELECTRIC CONSTANT
C     REINS=INSULATOR RELATIVE DIELECTRIC CONSTANT
C     T=INSULATOR THICKNESS IN ANGSTROMS
C     DA=IMPURITY DOPING LEVEL


      REAL*8 TITLE
      REAL*8 LABEL(4),TITEL(10,12),TITLEI(12),LABLE
      DIMENSION DA(20),DLOGDA(20),CMINH(20)
      N=13
      READ(5,2)(DA(I),I=1,N)
    2 FORMAT(10E6.1)
      READ(5,30)(LABEL(I),I=1,4)
   30 FORMAT(4A8)
      DO 100 I=1,5
      READ(5,31)(TITEL(I,M),M=1,12)
   31 FORMAT(6A8)
      DO 20 L=1,12
      TITLEI(L)=TITEL(I,L)
   20 CONTINUE
      READ(5,1) REINS,T,TITLE
    1 FORMAT(2F10.2,A8)
      WRITE(6,21)
   21 FORMAT('1')
      WRITE(6,7) TITLE,T
    7 FORMAT(' INSULATOR',A8,'WITH A THICKNESS OF',F7.0,
     1'ANGSTROMS')
      WRITE(6,6) REINS
    6 FORMAT('OINSULATOR RELATIVE DIELECTRIC CONSTANT',F7.1)


      DO 95 J=1,4
      READ(5,3) RESC
    3 FORMAT(F10.2)
      WRITE(6,8) RESC
    8 FORMAT(//,' SEMICONDUCTOR RELATIVE DIELECTRIC CONSTAN'
     1,'T',F7.1,/)
      WRITE(6,4)
    4 FORMAT(4X,'DOPING',/,5X,'LEVEL',2X,'C(MIN)HF',11X,
     1'XMAX',8X,'EG',3X,'2*DELEV',//)
      IF(J-3) 11,11,12
   11 MC=2
      IF(J.EQ.1) MC=1
      GO TO 13
   12 MC=3
   13 DO 90 K=1,N
      LABLE=LABEL(J)
      TEMP=300.
      VTH=8.625E-05*TEMP
      ES=RESC*8.85E-14
      X=0.0
      EG=0.181+4.52E-04*TEMP-0.568*X+5.8*X**4
      EMD=1.12*EG
      ENV=4.82E15*((TEMP*EMD)**1.5)
      EINS=REINS*8.85E-14
      DELEV=VTH*ALOG(ENV/DA(K))
      DELEV2=2.*DELEV
      XMAX=SQRT(2.*ES/1.6E-19/DA(K)*(EG-2.*DELEV))
      CSMIN=ES/XMAX
      CINS=1.0E08*EINS/T
      CMINH(K)=1./(1.+CINS/CSMIN)
      DLOGDA(K)=ALOG10(DA(K))-16.0
```

```
      WRITE(6,5) DA(K),CMINH(K),XMAX,EG,DELEV2
    5 FORMAT(1PE10.1,0PF10.4,E15.4,2F10.4)
   90 CONTINUE
      CALL DRAW(N,DLOGDA,CMINH,MC,J,LABLE,TITLE1,0.5,0.0,0,
     10,1,2,9,6,0,LAST)
   95 CONTINUE
  100 CONTINUE
      END
```

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13. ABSTRACT

A thorough understanding and a well developed fabrication procedure of MIS structures are the prerequisite for CCD applications. The object of this thesis is to study the narrow gap semiconductor MIS and investigate its feasibility for IR-CCI applications. Two MIS studies were made.

First, MIS of five lead-tin semiconductors were fabricated using E-gun evaporated 100-450A° thick Al_2O_3 or SiO_2 layers as insulators. C-V measurements indicated that these MIS behave qualitatively like that of Si-MOS. Accumulation, depletion and inversion layers were controlled by the gate voltage. However, comparisons of measured C-V with theoretical calculations did not yield quantitative agreement.

Second, MIS of 0.05Ω-cm p-type and 40Ω-cm n-type Ge were also studied. C-V and C-t measurements indicated standard MOS behavior although some small hysteresis was found. Analysis based on C-V data showed that the flatband voltage was approximately -1.2 volts and interface state density was on the order of 10^{13} /cm^2.

In addition, effects of electron bombardment simulating the space environment around Jupiter on a n-channel depletion MOSFET were studied. The negative threshold voltage was decreased and at a total dose of $2X10^{15}$ e/cm^2, it became positive making the MOSFET an enhancement type of very poor quality.

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Capacitive-Voltage Characteristics						
Charge-Coupled Devices						
Lead-Tin Semiconductors						
MIS Structures						

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